MPSOC ARCHITECTURAL DESIGN AND SYNTHESIS FOR REAL-TIME BIOMEDICAL SIGNAL PROCESSING IN GAMMA CAMERAS

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Abstract: In this paper, we propose an MPSoC architecture for implementing real-time signal processing in gamma camera. Based on a fully analysis of the characteristics of the application, we design several algorithms to optimize the systems in terms of processing speed, power consumption, and area costs etc. Two types of DSP core have been designed for the integral algorithm and the coordinate algorithm, the key parts of signal processing in a gamma camera. We implement our MPSoC architecture on FPGA, and synthesize DSP cores and Network-on-Chip using Synopsys Design Compiler with a UMC 0.18um standard cell library. The results show that our technique can effectively accelerate the processing and satisfy the requirements of real-time signal processing for 256 $\times$ 256 image construction.

1 INTRODUCTION

The growing demand for increasing sophisticated biodevices requires high-performance processing techniques. MPSoC (Multi-Processor System-on-Chip) is an ideal architecture for biomedical applications with its high throughput. With MPSoC, we can integrate multiple heterogeneous processors, hierarchy memory systems, custom logic, and on-chip interconnection to implement complex functions. Therefore, in the previous work, application-specific MPSoC architecture has been studied for biomedical applications. In (Khatib et al., 2006), a novel MPSoC architecture is proposed for real-time ECG (Electrocardiogram) analysis. By employing multi-issue VLIW DSPs with system interconnect from STMicroelectronics and commercial off-the-shelf biomedical sensors, the proposed MPSoC architecture can perform real-time ECG analysis with high sampling frequencies. In this paper, we propose an MPSoC architecture to solve real-time digital signal processing for gamma cameras, most commonly used medical imaging devices in nuclear medicine.

Gamma cameras generate images based on gamma radiation detection. PMT (PhotoMultiplier Tube) is one of the key components in a gamma camera which can detect fluorescent flashes generated by a crystal and produce current. Then the current and voltage are converted to digital signals by ADC (Analog to Digital Converter) behind a PMT, and finally images are obtained by processing the digital signals. To generate images, multiple PMTs are placed in hexagon configurations behind the absorbing crystal. In a typical scheme, a PMT array may consist of more than 30 PMTs. Using a serial 2D images obtained by gamma cameras from the different angles, 3D information can be acquired by SPECT (Single Photon Emission Computed Tomography).

To accelerate data processing, in current gamma cameras, DSP (Digital Signal Processing) boards based on PC platforms are widely used. With such platforms, typically, it takes about 15 - 30 seconds to generate one 64 $\times$ 64 image and 15 - 20 minutes to

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finish a complete scan in SPEC. The platforms can not efficiently produce higher-quality images such as 256×256. Their slow processing speed and big size limit the effective use of gamma cameras. The problem become particularly severe for portable gamma cameras (Sanchez et al., 2004; Sanchez et al., 2006) which work with nuclear radiation detectors with room-temperature. To improve image construction speed, a technique called PMT-PSPMT (Position Sensitive PhotoMultiplier Tube) (Jeong et al., 2004) is proposed. PMT-PSPMT is very effective in optimizing image construction times. But it reduces the image quality and cannot construct 256 × 256 image dynamically.

To solve these problems, we propose an MPSoC architecture for PMT data processing in a gamma camera. Our MPSoC architecture consists of the following four parts: one general-purpose embedded processor, a high speed data interface (HSDI), application-specific DSP cores and a Network-on-Chip with an interconnection bus. In the paper, we design two types of DSP core to implement two key algorithms, integral and coordinate, for real-time biomedical applications. We implement a prototype of our MPSoC architecture with FPGA, and synthesize DSP cores and Network-on-Chip using Synopsys Design Compiler with a UMC 0.18um standard cell library. The results show that our technique can effectively accelerate the processing and implement communication with small area cost. It can satisfy the requirements of real-time signal processing for 256 × 256 image construction.

The rest of this paper is organized as follows: in Section 2, we introduce necessary backgrounds related to gamma camera technique. In Section 3, we present the MPSoC system design. Section 4 presents the implementation of the prototype system. Section 5 provides the experimental results and discussions. In Section 6, we conclude the paper.

2 BACKGROUND

In this section, we provide an overview of basic knowledge related to gamma cameras. We first introduce the basic operating mechanism of gamma cameras and then present the algorithms used for image processing.

2.1 The Mechanism of Gamma Cameras

A gamma camera is a commonly used medical imaging device in nuclear medicine. In a gamma camera, images are generated by detecting gamma radiation. Basically, the counts of gamma photons that are absorbed by a crystal are accumulated, and the crystal produces a faint flash of light at the same time. The PMT array behind the crystal detects the fluorescent flashes and generates current. The current signal generated by the PMT is captured by the ADC, and two corresponding voltage signals are converted into digital signals. Digital signals are used to calculate the coordinate and energy of the gamma photons. With these coordinate and energy data, the final image can be produced.

2.2 Image-Construction Algorithms in Gamma Camera

During the whole medical imaging procedure, three algorithms, the integral, coordinate and amendment algorithms, are applied to the collected data.

The integral algorithm, as shown in Figure 1, is to calculate the energy of the voltage signal. In this algorithm, the serial data of each PMT is accumulated based on system status conditions.

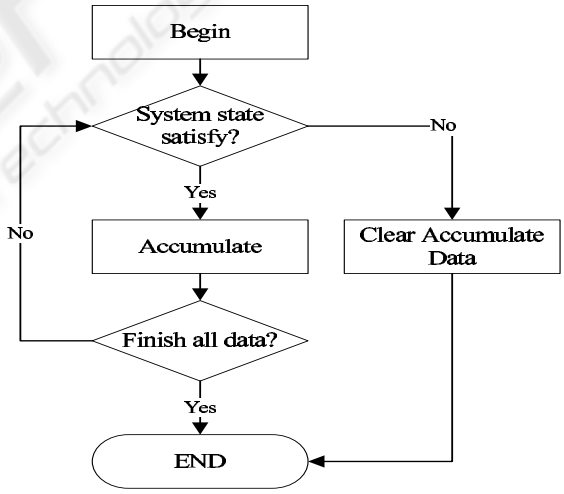

Figure 1: The integral algorithm.

The coordinate algorithm, as shown in Algorithm 2.1, includes the calculation for two parts, position and energy. In this algorithm, $P_1, P_2 \cdots P_m$ and $N_1, N_2 \cdots N_m$ are the internal data obtained from the two voltage signals, m is the count of the PMTs, and $T_1, T_2 \cdots T_m$ and $R_1, R_2 \cdots R_m$ are constant numbers. With these position and energy data, the gamma photon pulse can be determined. Then, an image can be constructed with a serial of the gamma photon pulse.
The amendment algorithm is used to amend energy

Algorithm 2.1 The Coordinate Algorithm.

Require: $P_1, P_2 \cdots P_m$,{ the internal data from the two voltage signal, m is the count of the PMTs}
$N_1, N_2 \cdots N_m$, { the internal data from the two voltage signals, m is the count of the PMTs}
$T_1, T_2 \cdots T_m$,{ constant numbers}
$R_1, R_2 \cdots R_m$,{ constant numbers}

1: $X_p \Leftarrow \frac{\sum_{i=1}^{m}(P_i \times T_i)}{\sum_{i=1}^{m} P_i}$, $Y_p \Leftarrow \frac{\sum_{i=1}^{m}(P_i \times R_i)}{\sum_{i=1}^{m} P_i}$, $X_n \Leftarrow \frac{\sum_{i=1}^{m}(N_i \times T_i)}{\sum_{i=1}^{m} N_i}$, $Y_n \Leftarrow \frac{\sum_{i=1}^{m}(N_i \times R_i)}{\sum_{i=1}^{m} N_i}$

2: calculate the position: $x \Leftarrow \frac{(X_p - X_n)}{(X_p + X_n)}$, $y \Leftarrow \frac{(Y_p - Y_n)}{(Y_p + Y_n)}$

3: calculate the energy: $E \Leftarrow \sum_{i=1}^{m} P_i + \sum_{i=1}^{m} N_i$

and position data with three table-lookup operations. This algorithm consists of two parts, energy and linearity emendation. After the data of every pulse is corrected by the correction table, a two-dimensional image of the relative spatial count density is constructed. With more pulse data, we can obtain more accurate image. To achieve that, multiple PMTs are placed in a hexagon array. In practical, a typical scheme usually uses 37 PMTs. The frequency of the pulse is limited to 1KHz in a typical gamma camera in order not to keep pulse data. Thus, with such a gamma camera, it takes about 15-30 seconds to build up one 64×64 image.

To reduce the image construction time, we can increase the pulse frequency of gamma photons. But with the limitation of the device, the maximum pulse frequency currently we can achieve is 500KHz-1 MHz. Correspondingly, we have to improve the speed of digital signal processing in order to generate image with such high pulse frequency. In this paper, our goal is to design an MPSoC architecture that can generate one 256×256 image in less than one second for gamma cameras with 1 MHz pulse frequency.

3 MPSOC SYSTEM DESIGN

In this section, we first introduce the MPSoC architecture in Section 3.1. Then we present issues related to general processors and HSDI in Section 3.2 and Section 3.3, respectively. Finally, the design of DSP cores and interconnection synthesis are discussed in Section 3.4 and Section 3.5, respectively.

3.1 Architecture Overview

Our MPSoC architecture is a typical heterogeneous multi-core architecture targeting on the application of gamma camera. It is specially designed for processing PMT data in parallel with multi-processors. In practice, fast image processing speed and high-quality image are the two of the most important performance metrics for gamma cameras. In order to achieve these goals, an MPSoC architecture, as shown in Figure 2 is proposed to speed up the image generation and improve image quality.

As shown in Figure 2, our MPSoC architecture consists of four parts: general processor, HSDI (High Speed Data Interface), DSP, and interconnection synthesis. Besides the four key parts, the MPSoC architecture also consists other components, e.g., the general embedded micro-controllers. In this architecture, the processor speed and the 32-bit on-chip interconnection are 200MHz, which are compatible with the 0.18um ASIC technology and the 32-bit bus interface IP cores. Next, we present the design issues for each key part of MPSoC architecture.

3.2 The General Processor

The general processor has one general purpose processor and some necessary IP cores, such as timer, UART, and SPI etc. Among these IP cores, the most important components are the on-chip RAM, SRAM/Flash controller, SDRAM controller and Ethernet MAC controller. The amendment algorithm and other general purpose computing are implemented in the general processor. The SRAM/Flash controller provides an interface to SRAM, ROM, NOR Flash and NAND Flash. The instruction code is stored in NOR Flash which is boot memory of the general processor. A reliable file system that stores the configurations using in the amendment algorithm is implemented in the NAND Flash. With an external Ethernet PHY chip, the Ethernet MAC controller is used to establish the communications with remote computers. In this way, the images and videos can be transferred to the remote computers through network, thus to help the doctors do some diagnosis. The on-chip RAM capacity is $512KB$ with 5 partitions. The first 2 partitions contain two amendment tables which are $256 \times 256 \times 16$ bit. The third partition contains one $256 \times 256 \times 8$ bit amendment table. The fourth partition contains the image constructed, which is 256 pixel $\times$ 256 pixel $\times$ 16 bit. The last partition is used as a high speed memory.

3.3 The High Speed Data Interface (HSDI)

The HSDI has a PMT data buffer and several LVDS (Low Voltage Differential Signaling) interfaces which

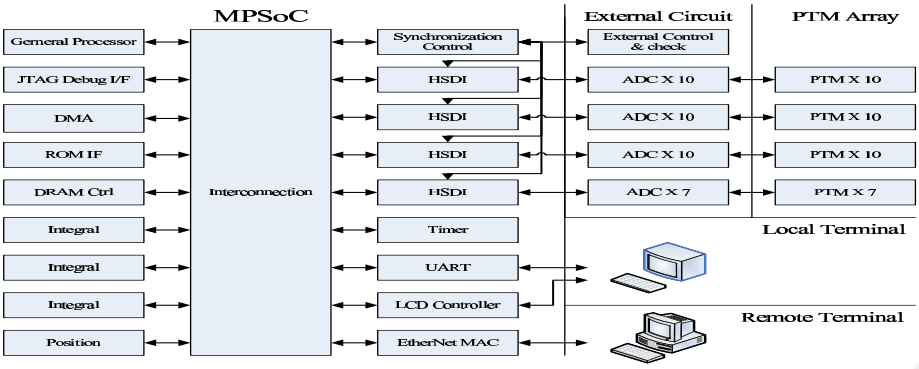

Figure 2: The MPSoC Architecture.

build a connection with external high speed ADCs. Since the sample speed of the ADC for PMTs is far lower than the processing time, buffers are used to store the PMT data of the external ADC. To exert the processing capability and diminish the interconnection area, the mount of the HSDI is determined by two factors: 1) the ADC sample speed; and 2) the on-chip interconnection speed. Usually, the common sample speed of the ADC for PMTs is 30MHz with the data width less than 16 bit, and the typical processor speed and on-chip interconnection with 0.18um technology and 32 bit width are 200MHz. Considering the bus arbitration cost, the maximum capacity of one HSDI is to take charge on 11 ADC data channels. For all of the 37 ADC data channels as discussed above, we use 4 HSDI as shown in Figure **??**(a) in which 3 of them take charge of 10 ADC data channels, and the last one takes charge of 7 ADC data channels.

3.4 The DSP Core Design

The customized DSPs used in our MPSoC architecture are designed for implementing the integral algorithm and the coordinate algorithm. We design two types of DSP, integral and coordinate, to implement the integral and coordinate algorithm, respectively. The corresponding block diagrams of the integral DSP and coordinate DSP are shown in Figure 3 and Figure 4, respectively.

The integral DSP has two bus interfaces, *Master* and *Slave*. The *Master* interface implements the data load/store, and the *Slave* interface implements the control and status logic accessing from other devices. The parameters for the integral algorithm are obtained through the *Slave* interface. Since there are 60 16-bit data for every gamma photons with two groups, upper and lower, which are implemented in the same integral algorithm, the data from HSDI is placed into the

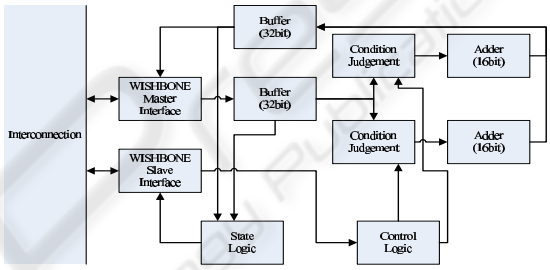

Figure 3: The Integral DSP.

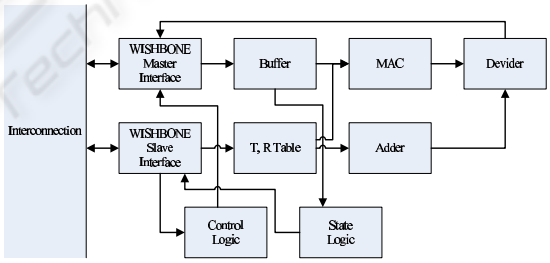

Figure 4: The Coordinate DSP.

buffer with 32-bit format, 16-bit for the upper group and 16-bit for the lower group. In other words, the integral algorithm is processed in parallel in the integral DSP. Thus, the integral DSP is designed with same units to accelerate the processing speed. For 30 PMTs data, the integral DSP uses 36 cycles to process them in which each integral DSP processes 10 gamma photons pulses within 2us. Thus, 4 integral processors are needed to process all of the 37 channel PMTs data.

The block diagram of the coordinate DSP is shown in Figure 4. The main components of the coordinate DSP are *MAC* (Multiply Accumulate) and *Divider*. The coordinate DSP has two bus interfaces, *Master* and *Slave*, which are as same as those of the

integral DSP. The *T* and *R* parameter tables are accessed through the *Slave* interface, and the data to be processed is placed in the buffer through the *Master* interface. As the *MAC* and *Adder* can work in parallel, we can process the numerator and denominator in algorithm 2.1 simultaneously. Since the throughput of the coordinate algorithm is much lower than the integral algorithm, only one coordinate DSP is required in the DSP design.

3.5 Interconnection Synthesis

As shown in Figure 2, interconnection serves the communication among DSP cores and other components. In most on-chip bus standards, such as AMBA(SPE, 2001), CoreConnect(SPE,), STBus(SPE, 2003) and WISHBONE(SPE, 2002), a share structure is used in the embedded processor. In the structure, the total bandwidth of the interconnection is limited to the bandwidth of each node since all buses are connected to one node and only one master can access the interconnection at one time. In order to fully utilize bandwidth, we need to perform careful analysis. In (Wang et al., 2007), we propose an interconnection synthesis algorithm to solve the problem.

4 PROTOTYPE IMPLEMENTATION

We have implemented the MPSoC prototype in an Altera Cyclone II FPGA EP2C35F672. In the implementation, we use the OpenRisc 1200 processor core as the general processor that runs at 20MHz which is 10% of the speed of the final ASIC implementation. We add one 512KB ZBT SRAM to our prototype since the on-chip RAM in Cyclone II FPGA can not meet our requirements. Besides the external SRAM, the prototype has 64MB SDRAM, 32MB NOR Flash ROM, 128MB NAND Flash ROM, 10M/100M Ethernet PHY, 640 $\times$ 480 16bit TFT LCD and other chips.

Table 1: The information for the prototype.

LEs	RAM(KB)	Multiplier(9-bit)
23468 (71%)	54 (92%)	16 (23%)
IO	PLL	Max Speed(MHz)
465 (98%)	1 (25%)	42

We test the prototype with input signals based on a real gamma camera, and check the output signals. The results show that it functions correctly. The numbers of resources we use are shown in Table 1. In this table, LEs denotes logical elements, RAM represents the on-chip-memory, and PLL denotes phase loop lock. The number inside the brackets for each resource represents the percentage between the number of resource we really use and the total number of resource provided by the system.

5 EXPERIMENTAL RESULTS AND DISCUSSIONS

To compare our MPSoC architecture with the general architecture, we have implemented the integral and coordinate algorithm both with an ARM9 processor and with our custom designed DSPs. In the experiment, we obtain the results of processing time, the area, RAM, power cost of our custom DSPs. For the interconnection, we have implemented our interconnection with WISHBONE protocol and our bus interconnection synthesis algorithm. We compare our technique with the crossbar and the reduce crossbar structure in terms of the area cost. In this section, we first present the results of processor comparison in Section 5.1, and then we present and analyze the results of interconnection optimization in Section **??**.

5.1 Processor Comparison

The typical sustaining time of the PMT reactivity electric current signal for gamma photons pulse is 2us. In this time interval, the ADC produces 60 data in which every 30 data is applied with the integral algorithm. The cycles and time for the integral and coordinate algorithm to process data that is produced within 2us are shown in table 2. We have tested the ARM9 program in SimpleScalar (Burger and Austin, 1997) and a hardware platform based on ARM 920T (ARM 920T, 2001) running with 203 MHz. The results are shown in Table 2.

Table 2: The testing results of ARM9 program in SimpleScalar and S3C2410.

	Condition	**Cycle**	**Time (us)**
The Integral Algorithm	SimpleScalar	2104	10.5
	S3C2410		21.6
The Coordinate Algorithm	SimpleScalar	1692	8.5
	S3C2410		24.2

In the table, we can see that it takes 2104 and 1692 clock cycles to finish the integral and coordinate algorithms, respectively, on the SimpleScalar simulator.

Based on the hardware platform, the times we need are 21.6 and 24.2 μs, respectively.

We design two types of DSP to implement the algorithms separately. In order to accelerate the processing speed, we use several integral DSPs with same design. The integral and coordinate DSPs are coded in Verilog HDL, and are synthesized to gate-level circuits using Synopsys Design Compiler and a UMC 0.18um standard cell library. The results generated by our technique is shown in Table 3. The comparison of the results generated using ARM9 and our customized DSP is shown in Table 4. From the table, we can see that our customized DSPs can preform with very high performance. With 5 integral DSP cores, we can achieve the requirements. The results show great performance improvement and cost reduction with our MPSoC architecture.

Table 3: The results with our DSP cores.

	Integral DSP	**Coordinate DSP**
Cycle	37	340
Time(us)	0.185	1.700
Area(um^2)	0.14	2.03
RAM(KB)	1	4
Power(mW)	18	264

Table 4: The comparison of the results from ARM9 and our DSP cores.

	DSP	**ARM920 Processor**
Quantity	5	197
Area(um^2)	2.59	1026.8
RAM(KB)	8	3152
Power(mW)	336	120

6 CONCLUSIONS

In this paper, we have proposed an MPSoC architecture for implementing real-time signal processing in gamma camera. Based on a fully analysis of the characteristics of the application, we designed several algorithms to optimize the systems in terms of processing speed, power consumption, and area costs etc. Two types of DSP core have been designed for the integral algorithm and the coordinate algorithm, the key parts of signal processing in a gamma camera. A prototype of our MPSoC architecture has been implemented with FPGA, and the test results show that it can function correctly. Various experiments have been conducted and discussed. We synthesized DSP cores and Network-on-Chip using Synopsys Design Compiler with a UMC 0.18um standard cell library. The results show that our technique can effectively accelerate the processing and satisfy the requirements of real-time signal processing for 256 $\times$ 256 image construction.

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