AUTOMATED SIZING OF ANALOG CIRCUITS BASED ON GENETIC ALGORITHM WITH PARAMETER ORTHOGONALIZATION PROCEDURE

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Abstract: This paper presents a method for the automated sizing of analog circuits using genetic algorithm (GA). For the rapid and efficient exploration of GA, we introduce the idea of search space sphering and dimension reduction with principal component analysis (PCA). The potential capability of the system is demonstrated through the automated sizing of wide-swing current mirror circuit. Experimental results show that the system with PCA successfuly generates higher-performance circuits under given evaluation function on average, and the dimensionally reduction method further improves the performance of solutions.

1 INTRODUCTION

Electronic design automation (EDA) has matured as a technology to be universally accepted for producing highly integrated VLSI systems. However, there still remain many difficult design problems to be addressed in the advanced SoC (System on Chip) era.

In this paper, we propose an automated analog circuit design method based on evolutionary computation. An analog circuit inherently involves tradeoffs among a large number of performance metrics and the performance is determined by the complex and nonlinear nature of relations between the topology and parameter values (e.g. device sizes) of a circuit. Therefore, the analog circuit design often requires simultaneous optimization of circuit topology and parameter values. It requires the knowledge and experience of experts who had trained in a particular way to understand circuit/device technologies. This is the major motivation to introduce evolutionary optimization techniques for the design automation.

There are already some approaches to the evolutionary design of analog circuit structures(Koza et al., 1997; Lohn and Colombano, 1999; Shibata and Fujii, 2001). The reference (Koza et al., 1997) describes various analog circuit design including analog filters and amplifiers by means of *genetic programming* (GP). The reference (Lohn and Colombano, 1999) proposes a method of representing electronic circuit structures by "linear representation" and its application to analog circuit synthesis using *genetic algorithm* (GA). The reference (Shibata and Fujii, 2001) also applies GA to the synthesis of analog circuits based on current path based coding. These approaches appear to perform both topology and parameter optimization equally. Both approaches have the possibilities of finding best possible solutions under given conditions and constraints since both topology and parameter optimization are performed simultaneously. However, the simultaneous optimization often leads to an explosion of search space, which requires much computation time for finding a solution, and sometimes converges into a local optimum.

To make our method suitable for practical use, we have proposed a two-stage optimization process of analog circuits as follows: (i) topology-oriented optimization using evolutionary computation and (ii) detailed optimization of parameter values (e.g. aspect ratios of transistors) using a commercially available automatic circuit sizing software(Homma et al., 2000; Homma et al., 2002; Natsui et al., 2005; Natsui et al., 2007). This storategy have achieved a reduction in the size of search space and an improvement in the search efficiency.

In this paper, we mainly focus on an automated analog circuit sizing for a given circuit topology by

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using GA. In order to accelerate the search efficiency of the circuit sizing system, we propose the idea of applying the parameter orthogonalization procedure based on *principal component analysis* (PCA) to the system. In the analog circuit design, the relative scale between circuit parameters such as the ratio of the length and width of a transistor or that of the widths of two transistors has an important role to determine circuit performance. If the system can consider the correlations between parameters that are specific to higher-fitness individuals and periodically reduce the search space, it can increase the search efficiency of the optimization process.

From this viewpoint, we introduce a search space reduction operation based on PCA. The principal component-based exploration realizes efficient parameter optimization, and additionally, dimensionality reduction method further reduces the search space. As a result, we can realize the high-performance optimization system which finds the optimal parameter set with less computation time.

The potential capability of the proposed system is demonstrated through the automated circuit sizing of a wide-swing current mirror, which is one of the most popular building block in analog circuit design. This paper is organized as follows: Section 2 presents the basic concept of the GA-based automated circuit sizing system and its extension using PCA. Section 3 demonstrates the experimental result. Section 4 is the conclusion and future prospects.

2 GA-BASED AUTOMATED CIRCUIT SIZING SYSTEM AND ITS EXTENSION USING PCA

2.1 Genetic Algorithm

Genetic algorithm (GA) can be regarded as a unique variation of evolutionary computation techniques (Back et al., 1997; Holland, 1975; Goldberg, 1989). In general, evolutionary methods mimic the process of natural evolution, the driving process for emergence of complex structures well-adapted to the given environment. The better an individual performs under the conditions the greater is the chance for the individual to live for a longer while and generate offspring. As a result, the individuals are transformed to the suitable forms on the designer's defined constraint.

Figure 1 shows the overall procedure of GA. At first, GA generates embryonic individuals randomly to form the initial population $P(0)$. Note that usually each individual is represented by a fixed-length bit string in the traditional GA, while our system applies *real-coded genetic algorithm* (RCGA) (Eshelman and Schaffer, 1993) which uses a real number vector representation of chromosomes.

```
program Genetic Algorithm;
 begin
  t := 0;
  {t: Number of generations.}
  initialize(P(t));
  {P(t): Population.}
  evaluate(P(t));
  while t ≤ Max. num. of gen. do
   begin
    C(t) := crossover(P(t));
    M(t) := mutation(P(t));
    evaluate(C(t) ∪ M(t));
    P(t+1) := select(C(t) ∪ M(t) ∪ P(t));
    t := t+1;
   end
 end.
```

Figure 1: Typical flow of GA.

The next step is to evaluate a fitness function of all individuals in $P(t)$. A value for fitness is assigned to each individual depending on how close it actually is to solving the problem. Since typical analog circuits have various performance metrics, an analog circuit optimization problem is usually formulated as (1) a single-objective optimization problem where different performance objectives are combined to form a scalar objective, or (2) a multiobjective optimization problem based on Pareto-optimality(Somani et al., 2007). In our system, we apply the single-objective approach for the system simplicity and reasonable computational effort. Thus a synthetic fitness function for a circuit is defined by the combination of fitness functions for various performance objectives.

After the evaluation, the system selects a set of individuals having higher fitness values to perform evolutionary operations: *crossover* and *mutation*. The crossover recombines two individuals into two new offsprings. The mutation operation, on the other hand, changes the values of chosen genes randomly. There are many ways how to do crossover and mutation. In our system, we apply blend crossover (BLX-α)(Fig. 2) and uniform mutation. Blend crossover generates the offspring vectors $X_1 = (x_{11}, x_{12}, \cdots, x_{1n})$ and $X_2 = (x_{21}, x_{22}, \cdots, x_{2n})$ from parant vectors $P_1 = (p_{11}, p_{12}, \cdots, p_{1n})$ and $P_2 = (p_{21}, p_{22}, \cdots, p_{2n})$ by $x_{1i} = \gamma p_{1i} + (1-\gamma) p_{2i}$ and $x_{2i} = (1-\gamma) p_{1i} + \gamma p_{2i}$, where $\gamma = (1+2\alpha)u_i - \alpha$, $u_i \in [0,1]$ is a random value. Uniform mutation, on the other hand, changes the value of the element to a value chosen from the uniform distribution on the specified interval.

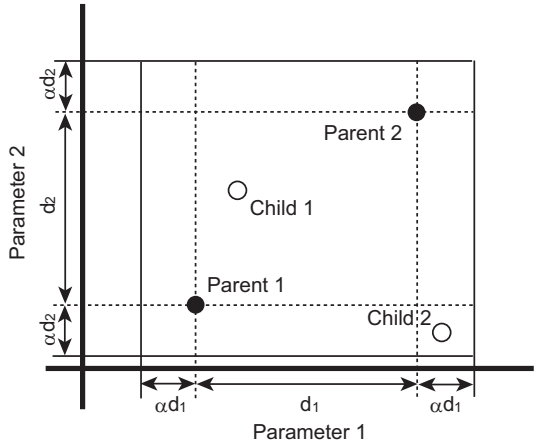

Figure 2: Blend crossover for two parameter vectors.

2.2 Search Space Reduction using PCA

Let us consider the search space reduction method of the automated analog circuit sizing on the basis of common characteristics of higher-fitness individuals. Given individuals which have averagely higher fitness values after a certain generations, one of the simplest way is to narrow down the search space of each parameter independently according to its mean and variance. If the parameters are orthogonalized and noncorrelated, this approach may work well. However in the case of analog circuit sizing, it sometimes fails and the exploration process converges to a local minimum since these parameters usually have strong correlations mutually. In order to perform effective search space reduction, we should apply an appropriate reduction method considering its relationship.

From this viewpoint, we utilize a coordinate transform procedure based on principal component analysis (PCA) to find a rotated orthogonal system such that the elements in the new coordinates are uncorrelated. PCA is a well known method for reducing the dimensionality by extracting components which are uncorrelated with each other, and has been used in a wide range of research including signal processing, statistics, and neural computing, as the powerful tool of data analysis and compression (Jolliffe, 2002). The exploration and search space correction based on the principal components and their variances have a possibility of enhancing the efficiency of the parameter optimization of GA.

The parameter orthogonalization procedure by PCA can be performed by the following steps:

1. Selects a set of higher-fitness individuals, where the parameter set corresponding to the ith individual is represented by $x_i = (x_{i1}, x_{i2}, \cdots, x_{iM})$.
2. Generates a parameter matrix
$$X = \begin{pmatrix} x_1 \\ \vdots \\ x_N \end{pmatrix} = \begin{pmatrix} x_{11} & \cdots & x_{1M} \\ \vdots & \ddots & \vdots \\ x_{N1} & \cdots & x_{NM} \end{pmatrix},$$
where each row corresponds a parameter set of an individual.
3. Generates a matrix $\tilde{X} = (\tilde{x_{ij}})$ by normalizing values of the matrix X so as to the mean $\mu_j = \frac{1}{N}\sum_{i=1}^{N} \tilde{x_{ij}} = 0$ and the variance $\sigma_j^2 = \frac{1}{N-1}\sum_{i=1}^{N}(\tilde{x_{ij}} - \mu_j)^2 = 1$ for each column.
4. Calculates a variance-covariance matrix, eigenvalues and eigenvectors of $\tilde{X}$.
5. Calculates an orthogonalized parameter matrix $X' = \tilde{X}A = (x'_{ij})$ where A is a matrix such that each column contains coefficients for one principal component.
6. Applies $x'_i = (x'_{i1}, x'_{i1}, \cdots, x'_{iM})$ to the parameter set corresponding to the ith individual.

The orthogonalization procedure is performed periodically with a specific interval during the evolution process by GA. This means that the system always use the vectors of real number elements with $\mu = 0$ and $\sigma^2 = 1$ for the individual representation, while the search space of circuit parameters is periodically corrected depending on the distribution of higher-fitness individuals. Additionally, if the variation of the last principal components are sufficiently small, we can eliminate these components from an exploration and reduce the length of individuals since they contribute relatively little extra information of individuals. This dimensionality reduction further improves the search efficiency, and reduces the total computational time.

When the system evaluates the evolved individuals, corresponding circuit parameters are restored by performing the above operation in reverse order (Fig. 3). Moreover, the restored parameters are quantized with a certain step depending on a variance of each parameter and the minimum step size of a target fabrication process. In our system, the parameters are quantized with step size $\sigma_j/10$, where σ_j is a variance of the jth parameter. If $\sigma_j/10$ is less than the minimum step size, the system applies the latter value. It realizes a coarse-to-fine search strategy, which achieves an effective exploration due to the prevention of the search space explosion of GA.

3 EXPERIMENT

We implement a GA-based automated analog circuit sizing system. The system applies GA to search the

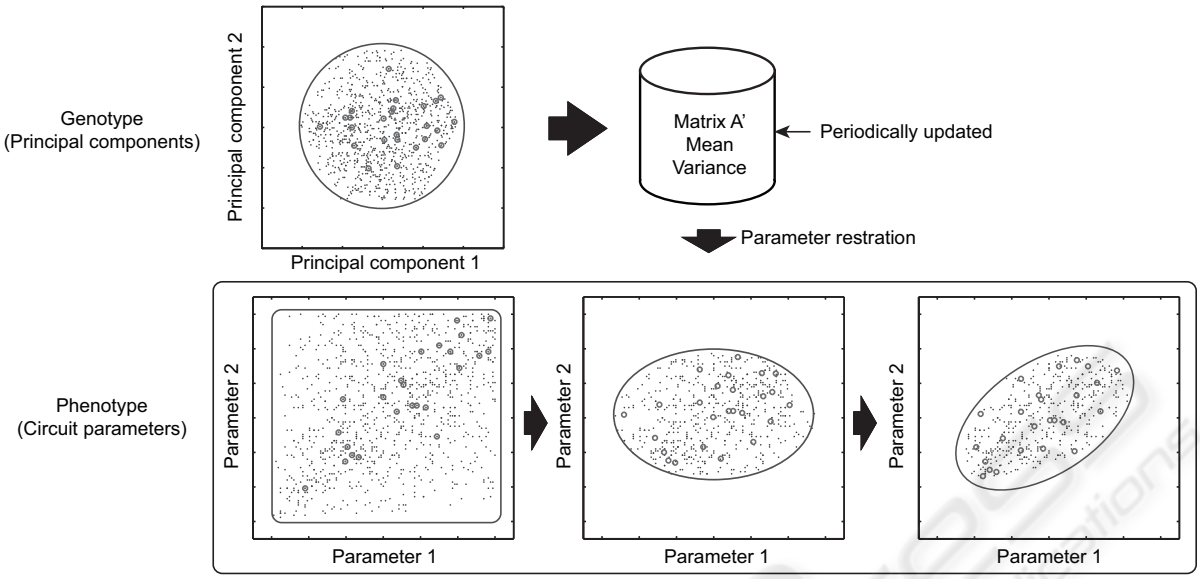

Figure 3: Parameter restoration (A' is a matrix such that $AA' = I$).

Table 1: Main parameter values for GA.

Parameter	Value
Maximum number of generations	500
Population size	200
Crossover method	BLX-0.5
Crossover rate	0.7
Mutation rate	0.1
Mutation method	Uniform
Selection method	Rank & Elitist
Interval of PCA execution	20
Num. of individuals for PCA	20

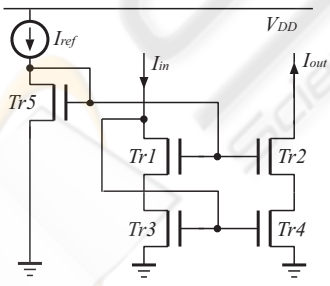

Figure 4: Wide-swing nMOS current mirror.

optimal set of circuit parameters (transistor length L and width W) which achieves higher performance on a given circuit topology, and periodically the orthogonalization procedure using PCA is performed to correct the search space of the optimization. After updating a characteristic vector matrix, the system destroys the lower-fitness individuals and creates randomly generated ones to form a population of the next generation.

The design specification considered here is a wide-swing nMOS current mirror (Fig. 4), which is widely used in analog integrated circuits both as a biasing element and as a load device for amplifier stage(Gray et al., 2001). The basic function of current mirrors is to produce an output current i_O equal to the input current i_I multiplied by a desired current gain B, that is, $i_O = -B \times i_I$. Ideally the gain B is independent of the input frequency, the output current i_O is independent of the output voltage v_O, the input voltage drop v_I equals zero, and the circuit area is as small as possible. In practice, the characteristics of real current mirrors deviate from those of ideal ones. There are various possible choices for a current mirror structure due to the trade-offs among the characteristics.

Design parameters of this circuit structure are (W_1,W_2,$\cdots$,W_5,L_1,L_2,$\cdots$,L_5), where W_i and L_i are the width and length of the MOS transistor Tr_i, respectively. The generated individual is translated into the corresponding netlist, which is simulated to analyze its electrical behavior and characteristics with SPICE simulations. Traditionally a weighted sum of the fitness functions has been used for the function aggregation. However, for nonlinear optimization problems like analog circuit sizing where the different objectives have nonlinear dependence upon each other, this approach sometimes causes some difficulties and leads to the premature convergence of the evolution process. For example, if one objective is easier to attain a target performance than other objectives, the

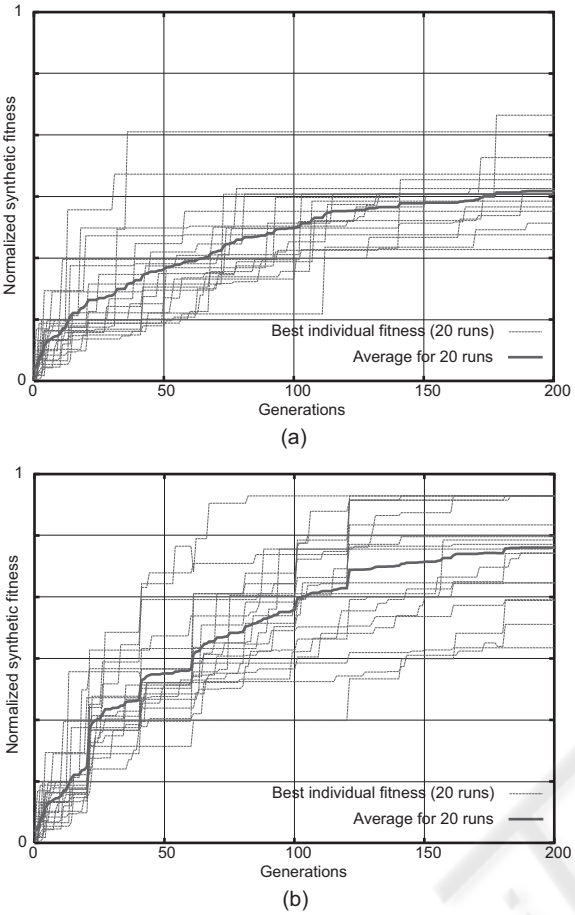

Figure 5: Fitness transition: (a) the conventional system, (b) the proposed system with PCA (The synthetic fitness values are normalized into $0 \leq F \leq 1$).

population sometimes converges to the specific search space, which leads to the evolutionary stasis. For satisfying all the objectives at the end of the optimization run, all the different fitness functions must be normalized and weighted equally.

In order to prevent the system from the premature convergnce, we define the synthetic evaluation function F as follows:

$$F = \prod_{i=1}^{3} F_i,$$

where F_1 evaluates the accuracy in i_I-i_O characteristic, F_2 evaluates the output saturation voltage investigated through DC transfer analysis, and F_3 evaluates the input impedance. The value of F_i is determined according to the rank of the ith characteristic in a population and is normalized into $0 \leq F_i \leq 1$. Thus the optimization process advances towards searching a parameter set which realizes higher performance synthetically. Note that only when the ith characteristic of an individual cannot be simulated by SPICE, F_i is set to 0 and the synthetic fitness value of the individual is also set to 0, which will be eliminated in the selection operation.

For more effecient exploration, we need further investigation of finding more proper fitness function. The result would be reported in the future.

In order to demonstrate the specific advantage of the search space reduction using PCA, we carry out experiments on generating an optimal parameter set of the given current mirror circuit structure. Table 1 summarizes the system parameters in this experiment. We set $0.6\mu m \leq W_i \leq 60\mu m$ and $0.6\mu m \leq W_i \leq 60\mu m$, and the minimum step size of these parameters is $0.1\mu m$. Thus the size of the possible choices is $(\frac{60-0.6}{0.1})^{10} \simeq 5.47 \times 10^{27}$, which needs 93 bits for an individual representation in traditional GA. By applying parameter quantizetion method described above, on the other hand, the proposed system limits the size to 10^{10} at most, which needs 34 bits, and the possible choices of circuit parameters are changed depending on the result of PCA.

Figure 5 shows the effect of PCA-based search space reduction by comparing the average fitness transitions. The system with PCA shows the tendency to improve the fitness more rapidly. It clearly shows that the proposed system explores a search space and finds better implementations more effectively compared with the conventional system.

Next, we evaluate the effect of applying PCA on the performance of evolved solutions. Figure 6 compares the performance of evolved circuits on

(a) the conventional system,

(b) the system with the search space reduction according to their means and variances independently,

(c) the system with the parameter orthogonalization procedure by PCA,

(d) the system with the parameter orthogonalization procedure and dimensionally reduction using PCA.

We performed 20 distinct evolutionary runs for each condition. We can see that the system with PCA generated higher-performance circuits under given evaluation function on average, and the dimensionally reduction method further improved the performance of evolved solutions.

In the following, we analyze one successful evolutionary process in detail. Figure 7 depicts an example snapshot of the evolved best fitness individual on each generation. The transistor sizes of them are described graphically. Given the initial random population, the system searches the set of parameters having higher fitness value for a while. At the 31st

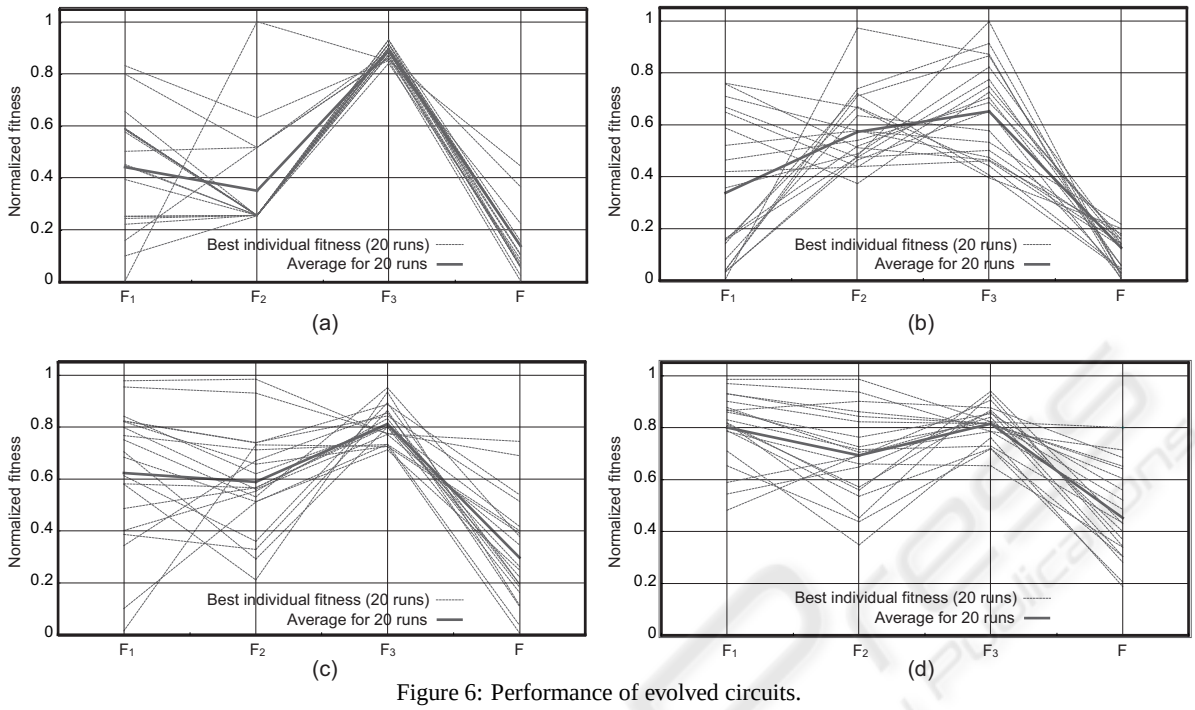

Figure 6: Performance of evolved circuits.

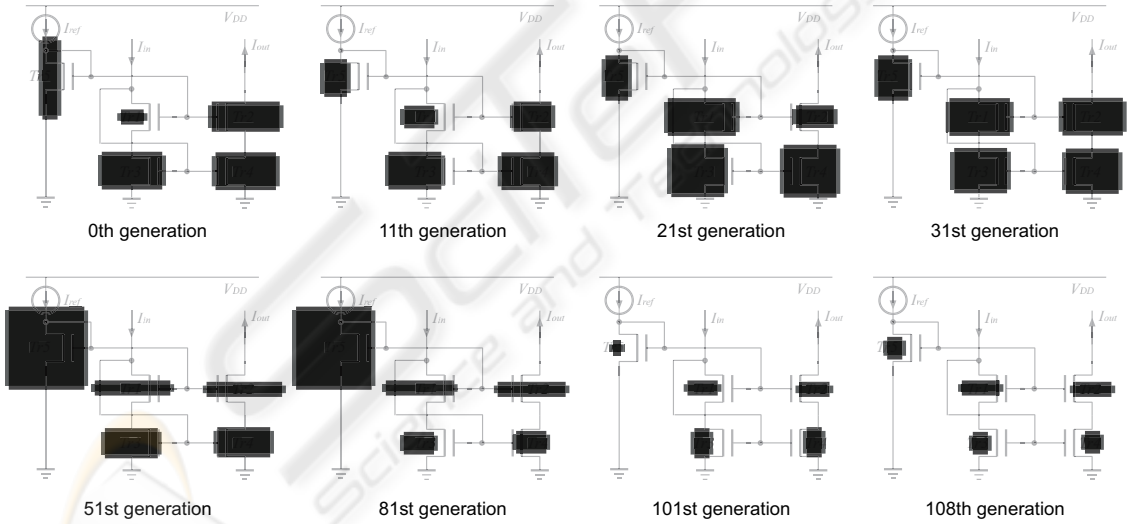

Figure 7: Best fitness individual transition.

generation, the system finds a set of parameters such that $(W1, L1, W3, L3) = (W2, L2, W4, L4)$, which is known as the proper setting of this structure. After that, the evolution process further improves the performance by changing a set of parameters. We can see that the best fitness individuals after the 31st generation have a tendency of keeping the above ratio since the parameter orthogonalization procedure is periodically performed to correct the search space. And finally, the system reaches the optimal solution at the 108th generation. This result shows that the PCA-based search space correction method works well and the system can find the optimal solutions effectively.

4 CONCLUSIONS

In this paper, we have presented a possibility of the GA-based analog circuit sizing system and its performance improvement using PCA-based orthogonalization procedure. An experimental synthesis of a wide-swing current mirror circuit demonstrates the poten-

tial capability of the proposed system to optimize analog-digital-mixed architectures without using expert knowledge of transistor-level circuits.

The experimental result also suggests a possibility of constructing intelligent circuit synthesis systems, which may evolve its ability by accumulating design experience. By introducing the guidelines for reusing suitable individuals, the proposed system could achieve more significant results.

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