Optimization of Digital Wireless Transceiver Embedded System Built on Xilinx FPGA

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Abstract. FPGA is becoming the most popular technology for developing new wireless systems. It makes design flow easier to realize even in a small company or academic institution with limited resources (human and/or budget). But when system is ready to enter production stage some drawbacks may stop its further progress. A short description of the wireless transceiver project for mobile vehicles is presented. Drawbacks are highlighted. The most critical of them, that reduces market attractiveness, is cost. To reduce cost a decision has been made to replace expensive Virtex4 by cheaper Spartan3 FPGA. This required making some changes in architecture. But the most part of previously created software and firmware were reused in new design.

1 Introduction

Today we can see a rapid growing market demand of high-rate wireless communication lines for mobile vehicles: cars, trains, ships, even more for unmanned vehicles. This communication line could be used to create ad-hoc type networks. Typical requirements for wireless transceivers of this communication line are following:

- Data rate up to 10 Mbits per second for uplink (to base station or control site);
- Data rate up to 100 kbits per second for downlink (control commands to mobile vehicle);
- Traffic types: high resolution color video, voice, control commands and telemetry;
- Vehicle speed from 0 up to 1000 km/h.

Existing and successfully selling technologies such as WiFi and WiMAX were tried to solve the problem but they do not fit requirement and are unusable. Fast movement of communicating objects causes OFDM signal structure totally degraded. Mobile WiMAX is not stable for today also. These technologies are too complex and have excessive functionality for asynchronous managed or ad-hoc networks. Furthermore implementations of WiFi and WiMAX modules presented at the market do not allow measuring power and other characteristics overload baseband and network layer logic required for cross layer optimization.

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Worth mentioning that flexible and energy efficient ad-hoc networks needed cross layer interaction, another words, tight communication between baseband processing and software implementing network management should be enabled.

The challenge we have stated to ourselves is to create wireless digital communication line for mobile vehicles with parameters and characteristics described above.

2 Existing System

There is a short description of currently existing wireless transceiver that was designed at our labs. The transceiver uses super heterodyne architecture that implemented in two parts: analogue front-end and digital baseband processing coupled with control unit based on embedded system with embedded Linux OS running on PowerPC 405 CPU (Fig.1).

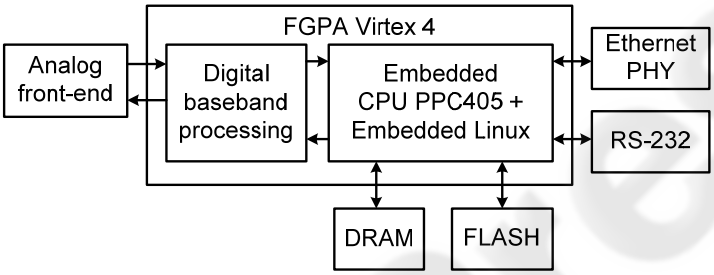

Fig. 1. Wireless transceiver embedded system.

Analog front-end made as digital-IF heterodyne architecture [1] and is presented on Fig.2. This architecture has some advantages and disadvantages:

Pluses.

- only single channel ADC and DAC are used,
- quadrature modulation/demodulation is in digital domain,
- absence of quadrature imbalance due to demodulation made in digital domain.

Minuses.

- high sample rates and dynamic range of AD/DA converters is required to digitize IF,
- extra band pass filtering stage (BPF2) for image rejection,
- reduced ability of miniaturization due to a big amount of external components.

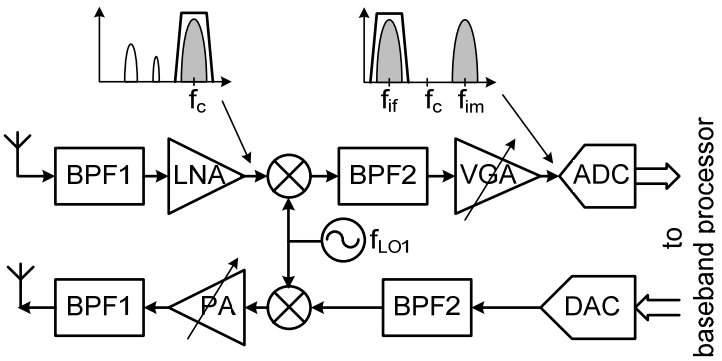

Fig. 2. Wireless transceiver analog front-end. f_c – carrier frequency; f_{if} – intermediate frequency; f_{im} – image center frequency; f_{LO1} – local oscillator frequency.

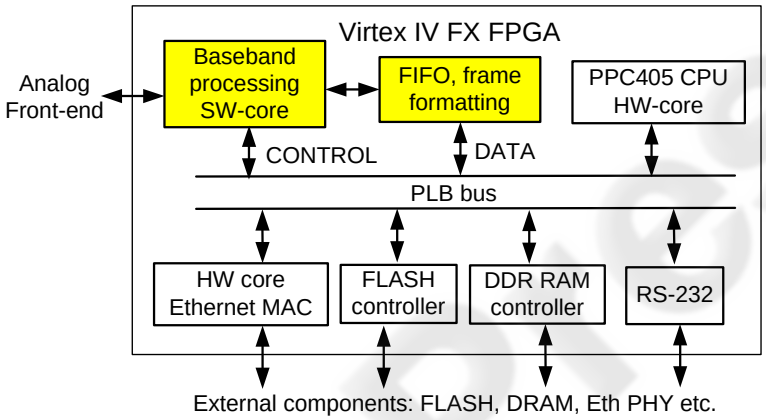

Fig. 3. Existing embedded system architecture for wireless transceiver based on Xilinx Virtex IV FPGA.

Main drawback of described transceiver is its cost. Main part of the transceiver is a Virtex 4 FPGA. This FPGA is very comfortable for engineer and is as flexible as it allows changing design and debugging in a very simple way. However, the price of Virtex 4 is few thousand dollars and it really disappoints potential customer.

Another one disadvantage is high sample rates of converters and additional bandpass filter stage for image rejection. The SAW filters are used in this architecture. They are expensive too and can not be used in reconfigurable SDR.

3 Modified Transceiver Architecture

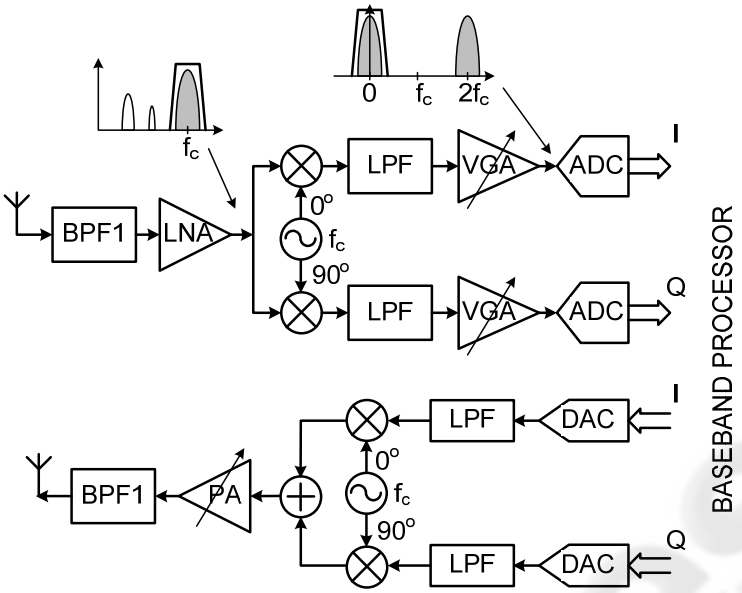

Fig. 4. Modified analog front-end architecture.

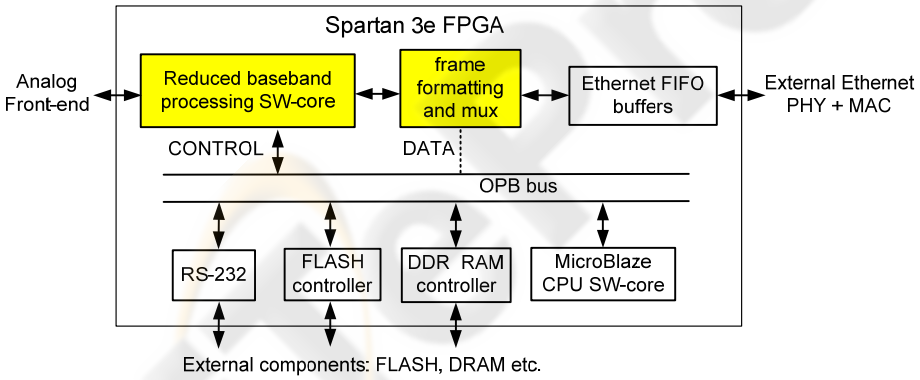

Fig. 5. Modified embedded system architecture for wireless transceiver.

As it can be seen after replacement of Virtex4 FPGA with Spartan3 embedded processor and peripheral bus are also changed from Power PC 405 hard-IP and PLB-bus to MicroBlaze soft-IP and OPB-bus. Fortunately there is Linux kernel and drivers for both architectures [2]. But we need to find proper Linux distribution for embedded Xilinx MicroBlaze CPU. A number of Linux embedded distributions are presented in Table 1.

Table 1. Embedded Linux Distributions supporting Xilnx FPGA embedded CPUs.

Name	URL	Supported CPUs	License	Real-time
ELDK	www.denx.de	PPC only	free	soft
Petalinux	www.petalogix.com	MB only	free	?
BlueCat	www.lynuxworks.com	both	commercial	soft/hard
MontaVista	www.montavistalinux.com	both	commercial	soft/hard
WindRiver	www.windriver.com	both	commercial	soft/hard

As we decided too reduce cost we refused commercial Linux distributions such as BlueCat, MontaVista and WindRiver. PetaLinux is the best choice for us. Unfortunately it does not have any real-time support. Possible solution is to use another SW platform, Quantum Leaps [3], for example. But major code revision will be required even more totally new code should be created.

Currently a novel ad-hoc network architecture is under development. One of the challenges we faced is to reduce real-time requirements of this network protocol. To determine what degree of real-time is requred the ad-hoc network immitation should be evaluated. This network can be created with cheap Spartan FPGA based development kits like “Spartan 3A Starter Kit” [4] with embedded PetaLinux onboard.

4 Conclusions

Two different wireless transceiver architectures are described. The first one has critical drawbacks that blocked successful entering to the market. The main core of the transceiver is an embedded system built on FPGA. The solution is to replace more powerful but expensive Virtex4 by Spartan3 FPGA. Such replacement requires to make some architecture improvements that were found and now are being implemened. Also a novel methods and algorithms of ad-hoc networks managing can be verified on this platform. We expect that this architecture with novel ad-hoc networking will help us to start commercial producing and distribution.

References

1. Gianini, V., Craninckx, J., Baschirotto, A.: Baseband Analog Circuits for Software Defined Radio, Springer, Dordrecht (2008).
2. Xilinx Open Source Linux Wiki, http://xilinx.wikidot.com
3. Quantum Leaps Innovating Embedded Systems, http://www.state-machine.com
4. Spartan-3A Starter Kit, http://www.xilinx.com/products/devkits/HW-SPAR3A-SK-UNI-G.htm