A FULLY INTEGRATED CMOS SENSOR FOR PICO-CURRENT MEASUREMENT ON SOLID-STATE NANOPORE DEVICES

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Abstract: In this paper, an integrated high-sensitivity patch-clamp sensor is proposed to measure the ultra-low current variation of a solid-state nanopore device. This sensor amplifier consists of three stages: 1) a headstage, 2) a difference amplifier and 3) a unity-gain buffer. For the headstage, a resistive-feedback transimpedance amplifier is employed to convert the small current to a readable voltage. The addition of a programmable gain to the second-stage difference amplifier allows the maximum gain to be increased to 168dBΩ. This sensor is fabricated in a 0.35μm CMOS process and is tested with an 80nm-diameter solid-state nanopore. We present a detailed circuit analysis for the low-noise patch-clamp design and its noise measurement result in this paper.

1 INTRODUCTION

For decades, the patch-clamp technique has been utilized in electrophysiology and pharmacology to analyze ion channels in living cell membranes and to monitor the effect of drugs on their dynamics (Hamill, 1981). Lately, this technique is also being applied for single-moelcule DNA anlysis using both biological nanopores and solid-state nanopores (Branton, 2008). Figure 1 illustrates a conventional patch-clamp sensor, comprised of a headstage and a difference-amplifier stage, to monitor translocation of individual DNA moledules through the nanopore (Kim[1], 2010). Here, the recording electrode (E_{REC}) follows the command voltage (V_{CMD}) variation applied to the non-inverting input of the differential amplifier (A_1) due to its high gain. This leads to an electrical field between the *cis* and *trans* chambers which are filled with a buffered ionic (KCl) solution. Because the DNA backbone is negatively charged, it can be captured into the pore, passing from the *cis* to the *trans* chamber when a *trans*-side positive voltage is applied. When the DNA traverses the nanopore, the ionic currents carried by potassium (K+) and chloride (Cl-) ions decrease in the range of tens to hundreds of pAs. Figure 2 shows the cross sections of a biological nanopore and a solid-state nanopore.

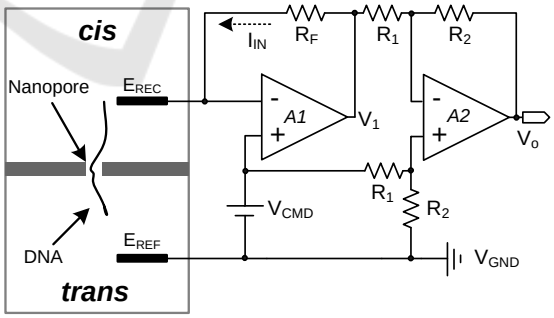

Figure 1: A conventional patch-clamp sensor to monitor DNA translocation events through the nanopore.

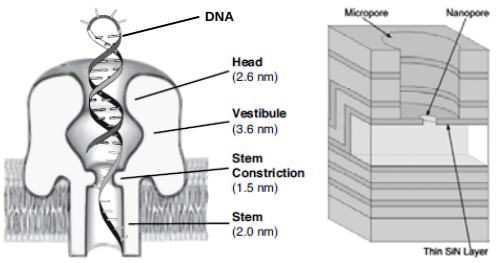

Figure 2: Biological nanopore using α-haemolysin protein (left) and soild-state nanopore using a silicon nitride layer (right). Here, the biological pore dimensions were found by crystallization (Song, 1996).

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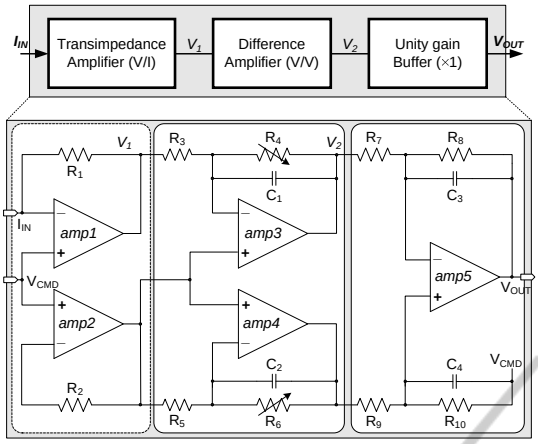

Figure 3: Proposed architecture of patch-clamp sensor.

To accurately monitor a DNA translocation event througth the nanopore and convert its minute current to a readable voltage range suitable for digitization, a high-senstivity transimpednace amplifier (TIA) is employed as the headstage of the patch-clamp sensor. For design simplicity resistive-feedback (rf) TIAs have been preferred to capacitive-feedback TIAs, which require a periodic reset (Prakash, 1989). In this work, we thus select an rf-TIA for the headstage.

Because the headstage makes a critical impact on noise of the patch-clamp sensor, its noise analysis and design parameters are consdiered in detail here, with the goal of achieving an ultra-low input-referred noise current. In addition to being low-noise, the patch-clamp sensor requires a high enough gain to amplify the small current signal. Use of a large feedback resistor in the TIA can increase the gain at the cost of chip area and bandwidth. Another way to increase overall gain is to add a programmable gain to the difference amplifier. More highly integrated parallel patch-clamp arrays (Fertig, 2002) enable multiple recordings as well as help save cost and time. For such high-density patch-clamp sensors, each sensing amplifier should dissipate low power.

In this work, we present the noise analysis and an integrated circuit realization of a patch-clamp sensor for solid-state nanopore applications. This sensor is tested with the solid-state nanopore device that was previously developed (Holmes, 2010).

2 SENSOR ARCHITECTURE

Figure 3 illustrates the proposed architecture of patch-clamp sensor composed of three stages: 1) headstage, 2) difference amplifier and 3) unity-gain buffer. For the headstage an rf-TIA is realized using an instrumentation amplifier topology that is capable of minimizing the input-offset voltage (Kim, 2011).

For the difference amplifier, a resistive feedback inverting amplifier having a gain of $-R_4/R_3$ is chosen. The observed DC variations in V_{out} are used to estimate nanopore conductance (S) (Healy, 2007). Here the adjustable resistors R_4 and R_6 provide a programmable gain, saving chip area by allowing use of a smaller feedback resistor in the preceding stage.

In order to drive pad, lead frame, pin, and probe parasitics, a unity-gain buffer is selected for the output stage. After the buffer an off-chip discrete high-order low-pass filter (LPF) is used to further restrict the patch-clamp sensor's bandwidth. In this work, a 5th-order Bessel LPF with a cutoff frequency of 10KHz is adopted.

3 CIRCUIT IMPLEMENTATION

3.1 Noise Analysis

In nanopore sensing, the principal noise arises from the nanopore device itself and the headstage. For the noise analysis, their simplified electrical models are illustrated in Figure 4. Here, R_N and C_N model the resistance and capacitance of the nanopore device. In the figure, R_E models contact and probe resistance, C_E arises from the double layer capacitance of E_{REC}. R_E is typically much smaller than R_N.

In terms of this equivalent circuit of the nanopore and E_{REC}, the thermal noise current of the nanopore and electrode is defined in Equation 1 (Kim^2, 2010).

$$S_N(f) = \frac{4kT}{\mathrm{Re}\left[X_N(f)\right]} \tag{1}$$

$$X_N(f) = \frac{\left(R_E + R_N\right) + j2\pi f \cdot \left(R_N R_E C_N + R_N R_E C_E\right)}{1 - \left(2\pi f\right)^2 \cdot \left(C_E C_N R_E R_N\right) + j2\pi f \cdot \left(C_N R_N + C_E R_E\right)} \tag{2}$$

$$S_H(f) \approx \frac{1}{R_1^2} \cdot \left\{ \frac{A(s) + A(s) \cdot sC_P \cdot R_1}{1 + A(s) + sC_P \cdot R_1} \right\}^2 \cdot \overline{V_{n,AMP1}^2} + \frac{1}{R_1^2} \cdot \left\{ \frac{A(s)}{1 + A(s) + sC_P \cdot R_1} \right\}^2 \cdot \overline{V_{n,R_1}^2} \tag{3}$$

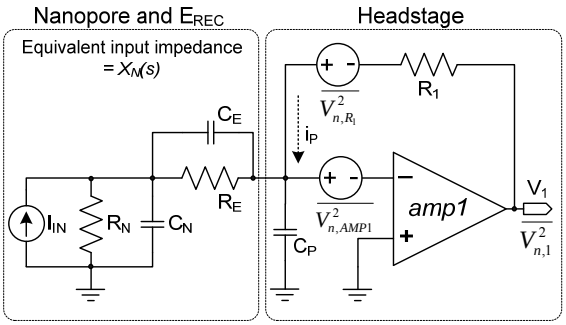

Figure 4: Simplified electrical model of nanopore, E_{REC} and headstage.

Here, k and T are the Botzmann constant and absolute temperature, respectively. The denominator of Equation 1, $X_N(f)$, denotes the impedance of the equivalent circuit which is expressed in Equation 2. Because DNA translocation events occur within a bandwidth of 10KHz and R_E is negligible compared to R_N, $X_N(f)$ is approximately equal to R_N at lower frequencies. Therefore, $S_N(f)$ is simplified to $4kT/R_N$ which is proportional to the conductance of the nanopore.

In addition to the noise current of the nanopore and E_{REC}, the input noise current of the headstage has a critical impact on the background noise because of its input-pair transistor's $1/f$ noise, which increases at lower frequencies. In Figure 4, $V^2_{n,AMP1}$ and $V^2_{n,R1}$ represent the input-referred noise voltage of the core-amplifier, *amp1*, and the thermal noise of R_1. The other stages' noise sources are ignored because of the relatively high gain of the headstage (Kim[1], 2010). Accordingly, the input-referred noise current of the headstage at lower frequencies is calculated in Equation 3.

The parameter C_P is the parasitic capacitance stemming from a coaxial cable, a BNC connector, a copper line on PCB, a lead frame, a pad, an ESD cell and input-pair transistors of the core-amplifier. $A(s)$ is the amplifier's transfer function, $A_0/(1+s/\omega_0)$, where A_0 and ω_0 represent its open-loop gain and bandwidth. $A(s)$ can be simplified to A_0 at lower frequencies. Thus, $1/A(s)$ in Equation 3 is neglected, leading to the simplified expression given by

$$S_H(f) \approx (2\pi f \cdot C_P)^2 \cdot \overline{V^2_{n,AMP1}} + \frac{4kT}{R_1} \qquad (4)$$

The second term in Equation 4 can be reduced by increasing R_1 at the cost of larger area and a limited bandwidth. To diminish the first term, $V^2_{n,AMP1}$ also has to be as low as possible.

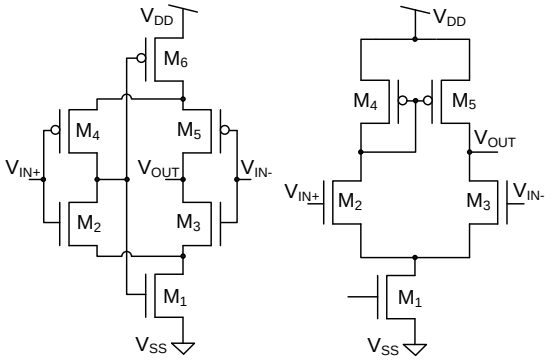

Figure 5: Self-biased differential Bazes amplifier (left) and general differential amplifier (right).

According to Equations 1 and 4, the background noise during the nanopore sensing is calculated as

$$S_B(f) \approx (2\pi f C_P)^2 \cdot \overline{V^2_{n,AMP1}} + \frac{4kT}{R_1} + \frac{4kT}{R_N} \qquad (5)$$

This noise equation shows that the thermal noise of the feedback resistor, $4kT/R_1$, is dominant compared with the nanopore noise, $4kT/R_N$ due to the usual situation where $R_N >> R_1$. Thus to lessen the overall background noise, a low-noise core-amplifier should be designed for the headstage.

3.2 Low-noise Core-amplifier Design

A self-biased differential Bazes amplifier (Bazes, 1991), shown in Figure 5 (left), is used for the low-noise core-amplifier design in this work. By virtue of the symmetric structure of NMOS and PMOS transistors, this amplifier is able to achieve both a symmetrical positive and negative input common-mode range (ICMR) and power-supply rejection ratio (PSRR). Its structure also enables a high gain because both the NMOS and PMOS contribute to the effective transconductance (g_m). Thus, its gain, $(g_{m2}+g_{m4})\times(r_{o3}\|r_{o5})$, where r_o denotes the transistor output resistance, is higher than the gain, $g_m\times(r_{op}\|r_{on})$, of a differential amplifier, as illustrated in Figure 5 (right), previously used (Weerakoon,2009). Dividing the output equivalent noise by the squared gain of the amplifier, the input-referred noise voltage of this Bazes amplifier is approximately:

$$\overline{V^2_{n,AMP1}} = \underbrace{\left[\frac{1}{(WL)_2} + \frac{1}{(WL)_4}\right] \cdot \frac{2K}{fC_{ox}}}_{1/f\ noise} + \underbrace{\frac{8kT\gamma}{(g_{m2}+g_{m4})^2}}_{Thermal\ noise} \qquad (6)$$

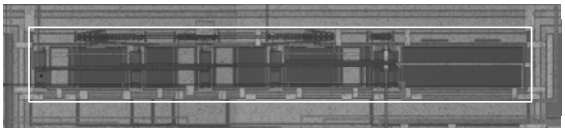

Figure 6: Chip micrograph occupying an active-die area of 980μm×121μm.

Here, K is a process-dependent constant on the order of $10^{-25}V^2F$. Because of the increased trans-conductance of this topology, the thermal noise term is smaller relative to a differential amplifier as well. The $1/f$ noise can be also reduced by enlarging $(WL)_2$ and $(WL)_4$. In this design, PMOS and NMOS input pair transistors, with aspect ratios of 72μm/1.5μm and 54μm/1.5μm, were used to reduce the $1/f$ noise.

4 TEST RESULTS

This patch-clamp sensor was fabricated in a 0.35μm 4M2P CMOS process and tested with an 80nm diameter solid-state nanopore device. Figure 6 shows a micrograph of this prototype chip which occupies an active-die area of 0.11858mm^2.

The patch-clamp sensor has programmable gains of 168, 161, 152 and 138dBΩ and accomplishes a balanced ICMR of $1V_{PP}$ which results from the symmetrical structure of the core-amplifier. When the gain is set to 168.2dBΩ, this amplifier consumes a maximum power of 437μW.

Using the solid-state nanopore we measured an open-channel current resulting from a DC variation of V_{CMD} across the nanopore conductance. Figure 7 displays the graph of the nanopore current verses voltage whose slope yields its conductance. The measured slope is 8.6nS and thus R_N is 1/8.6nS ≈ 116 MΩ.

Figure 8 shows the input noise spectral density of the patch-clamp sensor. Due to the high-order LPF, the noise dramatically decreases beyond 10 kHz. The input root-mean-square (RMS) noise current of this sensor is measured as 4.25pA at 10KHz bandwidth, which is low enough to monitor DNA translocation events that register tens of pA in magnitude. The overall performance of the proposed patch-clamp sensor is summarized in Table 1.

5 CONCLUSIONS

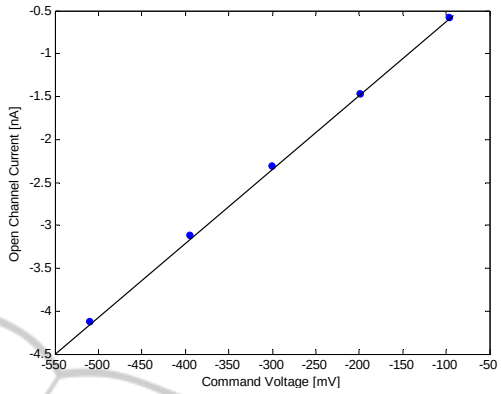

Figure 7: Measured open-channel current variations.

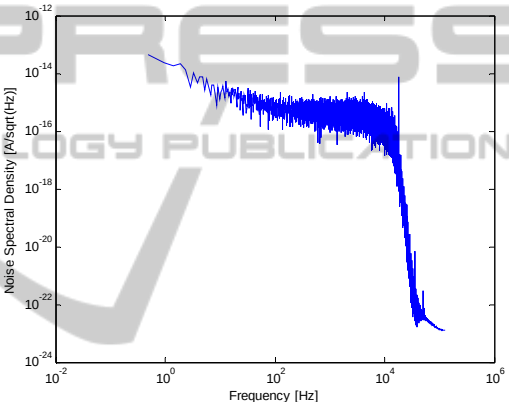

Figure 8: Measured input-noise spectra of the patch-clamp sensor.

Table 1: Summary of chip performance.

DC gains	168, 161, 152, 138dBΩ
Input-referred noise	$4.25pA_{RMS}$@168dBΩ
ICMR	$1V_{PP}$
Supply voltage	±1.5V
Max. power dissipation	437μW
Chip area	0.11858mm^2
Technology	0.35μm 4M2P CMOS

An integrated $4.25pA_{RMS}$-noise sensor has been designed for pico-current measurements on a solid-state nanopore device. To monitor the small current variation through the nanopore, a resistive-feedback transimpedance amplifier has been employed as a headstage with a programmable gain added to the second-state difference amplifier for additional gain. This proposed sensor operates from ±1.5V, has four different gains and consumes a maximum power of 437μW. This chip was fabricated in a 0.35μm 4M2P CMOS process and tested. Using an 80nm-diameter

solid-state nanopore, we measured the open-channel current variations, resulting in a nanopore resistance of 116 MΩ.

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REFERENCES

Hamill, O., et all, 1981. Improved patch-clamp techniques for high-resolution current recording from cells and cell-free membrane patches. *European Journal of Physiology*, vol. 391, no. 2, pp. 85-100.

Branton, D., et all, 2008. The potential and challenges of nanopore sequencing. *Nature biotechnology*, vol. 26, no. 10, pp. 1146-1153.

Kim[1], J., et all, 2010. An integrated patch-clamp amplifier for ultra-low current measurement on solid-state nanopore device. *IEEE international SoC design Conference*, pp. 424-427.

Song, L., et all, 1996. Structure of staphy-lococcal α-hemolysin, a heptameric transmembrane pore. *Science*, vol. 274, pp. 1859-1866.

Prakash, J. Paulos, et all, 1989. A mono lithic patch-clamping amplifier with capacitive feed- back. *J. of Neurosci. Methods*, vol. 27, no. 2 pp. 165-172.

Fertig, N., et all, 2002. Nanostructured suspended aperture for patch clamp recording and scanning probe application on native membranes. *Biophys. J.*, 78.

Holmes, M.R., et all, 2010. Micropore and nanopore fabrication in hollow antiresonant reflecting optical waveguides. J. Micro/Nanolith. *MEMS MOEMS*, vol. 9, no. 2, pp. 023004.

Kim, J., et all, 2011. On-chip patch-clamp sensor for solid-state nanopore applicat- ions. *Electronics Letters*, vol. 47, no. 15, pp. 844-846.

Healy, D., et all, 2007. Solid-state nanopore technologies for nanopore-based DNA analysis. *Nanomedicine* (Lond), vol. 2, no.6, pp. 875-897.

Kim[2], D., et all, 2010. Performance comparison of low current measurement system for biomedical applications. *in Proc. of IEEE Int. Symp. Circ. And Syst.*, pp. 3469-3472.

Bazes, M., 1991. Two novel fully complementary self-biased CMOS differential amplifiers. *IEEE J. of Solid-State Circuit*, vol. 26, no. 2, pp. 165-168.

Weerakoon, p., et all, 2009. An integrated patch-clamp potentiostat with electrode compensation. *IEEE Trans. Biomed. Circ. And Syst.*, vol. 3, no. 2, pp. 117-125.