A 0.18μm CMOS 2nd Order Sigma-Delta Modulator for Low-power Biosensor Applications

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Abstract: Silicon biosensors are becoming increasingly popular for the study of cell growth and movement in biological systems. These biosensors need small, low power, highly accurate sensors and analog to digital converters (ADCs) in order to generate chemical images of small tissue samples. Low-power and low-voltage design is key in battery operated systems, and the size of the circuits need to be kept small such that arrays of sensors can be placed on each chip. This paper presents a low-voltage, low-power, 2nd order Sigma-Delta modulator for use in an electrochemical biosensor system. The modulator was designed using a commercial 0.18μm CMOS process with a supply voltage of 0.9V. With an input signal bandwidth of 1kHz it achieves a SNDR of 61.2dB using an over-sampling ratio of 500. Power dissipation is 165μW and it occupies 0.0225mm^2 of silicon area.

1 INTRODUCTION

Integrated silicon biosensors have been proposed as a method for detecting chemical levels within biological systems (Pettine, 2012). One application for these biosensors is the study of cell movement and development within brain tissue. Using electrochemistry for signal detection, an array of micro-electrodes in such a biosensor would be able to measure chemical gradients across small pieces of living tissue. These gradients form a chemical image. Current methods for creating chemical images involve dye and marking compounds which could kill the tissue sample. The traditional methods of observing cell movement and changes are not ideal because temporal changes in chemical concentrations and cell movement cannot be observed reliably. An integrated silicon biosensor array of hundreds or thousands of electrodes would solve these problems by measuring chemical levels in live tissue, allowing scientists to observe important changes over time.

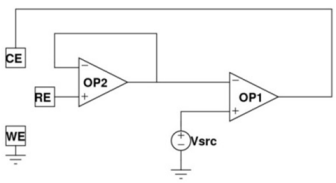

Figure 1: Potentiostat schematic.

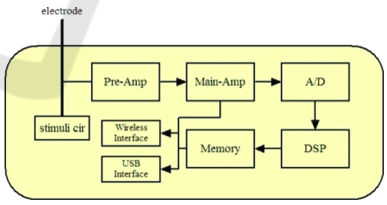

Figure 2: The top-level schematic of the biosensor system.

Nitric oxide (NO) is a chemical that is believed to influence cell movement and growth in brain tissue. This chemical is electrochemically active and can be measured using electrochemical methods implemented in a silicon biosensor. In order to create the chemical image of the NO in the tissue, many circuit components are needed. First, a potentiostat is used to induce a current in the tissue sample proportional to the concentration of nitric oxide. A low power design of the integrated potentiostat for this system can be found in (Duwe, 2011). The induced currents are extremely small, on the order of tens of picoamps, and need to be converted to voltage signals and amplified by way of a transimpedance amplifier. Finally, main amplifiers and an analog to digital converter (ADC) further amplify the signal and convert it to a digital value. A low power bit-serial decimator design that interfaces with the modulator presented in this paper can be found in (Scholfield, 2012). Figure 1 shows the electrode arrangement and potentiostat circuit proposed in (Duwe, 2011), and Figure 2 shows

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the top-level schematic of the biosensor system.

In order to create an accurate chemical image, the electrodes need to be spaced at distances comparable to the size of individual cells within the tissue sample. Electrode pitches of 10μm to 25μm are desirable. Ideally, each electrode should have its own dedicated circuitry; however with the extremely small electrode pitch this is not realistic. Regardless, minimizing the area of the circuitry is important to reduce the number of shared electrodes per circuit block. Likewise, power consumption should be minimized since the biosensor will contain many copies of the detection circuitry running in parallel. Power consumption must also be limited to avoid heat build-up within the tissue, possibly causing damage.

The chemical signals detected with the potentiostat typically have very low bandwidths; nitric oxide signals do not normally exceed 1 kHz. While bandwidth requirements are low, measurement accuracy is much more important. Noise and signal distortion must be avoided to preserve the integrity of the small signals inherent in bio-electric systems. Sigma-Delta ADCs are ideal for biosensor applications because they inherently have higher resolution and lower bandwidth than other ADC topologies.

Many different designs for low-power Sigma-Delta Modulators have been presented. The designs in both (Zhang, 2010) and (Jasutkar, 2011) are based on 0.18μm CMOS processes with nominal 1.8V power supplies. These designs use standard architectures and standard techniques for reducing power. The design in (Zhang, 2010) was intended for audio applications, while (Jasutkar, 2011) presents a design for biomedical applications such as electocardiograms. The designs presented in (Goes, 2006) and (Lee, 2006) also use 0.18μm CMOS processes but they use supply voltages of 0.9V and 0.8V respectively to reduce power. Besides lowering the supply voltage, these designs modify the standard architecture to save power. (Goes, 2006) shares a single op-amp between multiple integrator stages and (Lee, 2006) is able to be used at different speeds depending on the application to maximize efficiency. The design presented in this paper explores the efficiency of using a reduced power supply to lower power consumption while still using a standard, easy to implement architecture.

All of these designs are also fully differential architectures while the proposed design is single ended. The use of differential design has the advantage of expanded output range; however, our application focuses on NO which has a narrow activation range. Therefore, a single-ended design is chosen for reduced silicon area. In switched-capacitor circuits where capacitors can occupy a large percentage of the total area, this is critical. Section II of the paper will detail the design of the modulator and its components, and Section III will cover the proposed physical layout and present simulation results.

2 PROPOSED LOW POWER MODULATOR DESIGN

2.1 Top Level Design

The overall block level diagram of the proposed modulator is shown in Figure 3. The design is implemented using a standard 0.18μm silicon process and a supply voltage of 900mV. The overall topology is a single ended, second order, Sigma-Delta modulator. This topology uses two integrators, a comparator, and a 1bit DAC to provide feedback. With accuracy and

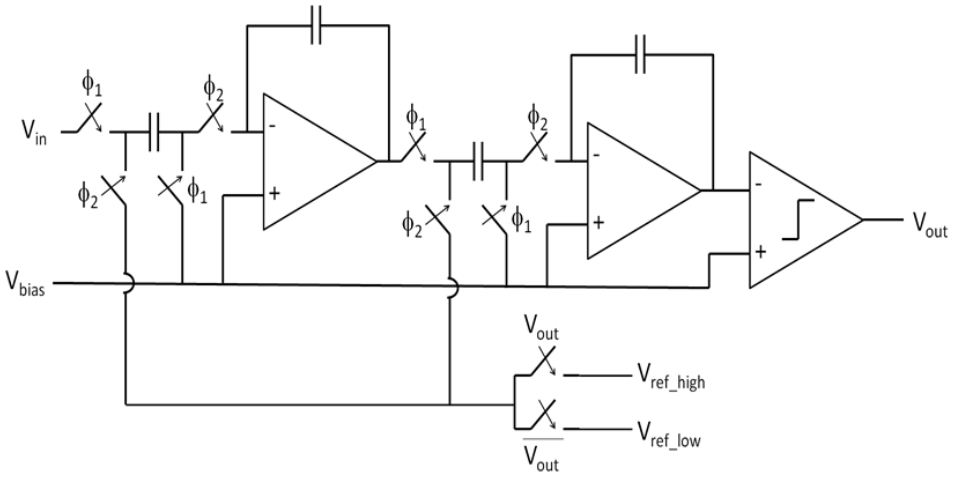

Figure 3: Top level modulator schematic.

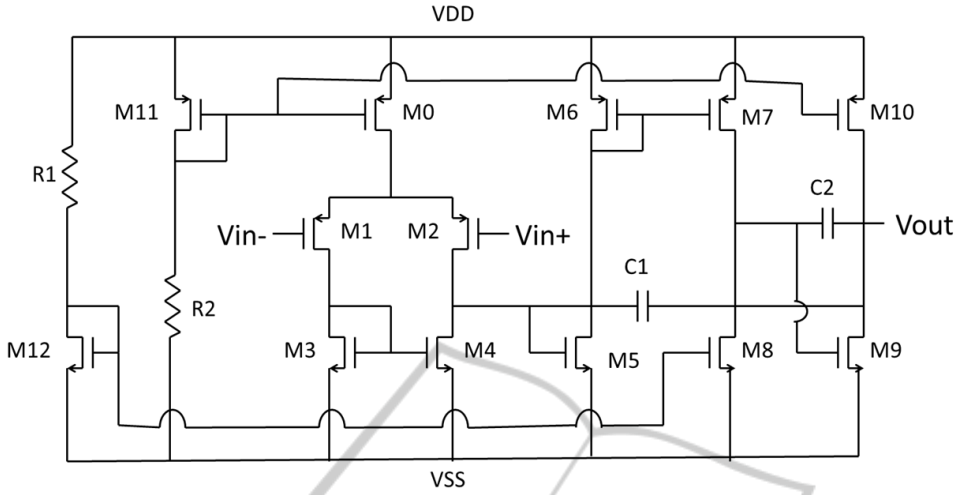

Figure 4: Op-amp schematic.

power consumption prime concerns in this design, the modulator is implemented using switched capacitors which both improve matching in the integration stages and allows for lower power consumption than a continuous time resistive implementation.

The bio-chemical signals the chip will be measuring have a maximum bandwidth of 1kHz which makes a Sigma-Delta based ADC with a large oversampling ratio ideal for accurate measurements. The input is sampled at 1MHz resulting in an oversampling ratio of 500. This clock frequency was chosen based on the performance requirements of the decimation filter presented in [3], and power consumption was reduced as much as possible using this sampling rate.

2.2 Modulator Op-amp Design

The schematic for the proposed op-amp is shown in Figure 4. The nominal supply voltage used with this process is 1.8V because the threshold voltages of the nFETs and pFETs available in this process are approximately 450mV and -400mV respectively. When designing with a 900mV supply, cascoding transistors is not practical in most situations. Thus the op-amp uses multiple, simple, stages to achieve high gain.

The design features three stages comprised of a differential pair input followed by common source amplifiers and current mirrors. Adding extra stages to an op-amp inherently leads to stability problems, and thus two large compensation capacitors are needed to maintain a reasonable phase margin. Capacitors C1 and C2 in the schematic have values of 3.6pF and 1.3pF respectively. Because of the relatively large values of the compensation capacitors they are implemented on using poly/n-well capacitors. These capacitors are used because they are much more area efficient than standard metal/poly capacitors. The differential pair uses pFETs for the input to reduce noise, and the input/output common mode voltage is set to 175mV. With the limited supply voltage, the maximum peak-to-peak output swing is 300mV. Internal biasing voltages for nMOS and pMOS devices are generated using simple current mirrors with resistors generating the reference currents. The resistors are implemented as thin-film devices which are more area efficient and more accurate than other resistor technologies. Monte Carlo simulations have shown that these bias voltages do not vary widely enough to impact the functionality of the op-amp.

Small bias currents were used throughout the op-amp to reduce power consumption. All branches in the op-amp use 10μA bias currents except the output stage which uses 30μA to aid in stability. In total, the op-amp uses 70μA of current and consumes 63μW. The proposed design has a DC gain of 112dB, 8.3Hz -3dB bandwidth, and a phase margin of 77 degrees.

2.3 Integrator

The proposed modulator uses two switched capacitor integrators which each use a 100fF sampling capacitor and 4pF feedback capacitor. The sampling capacitor uses bottom plate sampling to reduce error due to charge injection. The ratio of feedback capacitance to sampling capacitance is set to 40:1 to prevent the output of the first modulator from saturating. Using this ratio the output of the first modulator uses the entire 300mV peak-to-peak output swing range of the op-amp. The capacitance ratio of the second integrator was set to 2:1, which allowed the second integrator to use its full output range as well.

While the capacitance ratio is determined by the output swing requirements of the op-amps, the absolute sizes of the capacitors are chosen based on a compromise between noise characteristics and physical size when implemented on chip. The 100fF input capacitor was chosen because it is the smallest value possible which meets the thermal noise requirements of the ADC system.

The sampling capacitor uses a poly/metal capacitor which is extremely linear but also very large. The feedback capacitor, which is much larger, is implemented with a poly/n-well capacitor which has nonlinear properties yet is very area efficient. Obviously, using different types of capacitors makes matching more difficult, but the savings in area is considerable compared to using two poly/metal capacitors. Poly/n-well capacitors are roughly nine times smaller than poly/metal capacitors.

2.4 Comparator Design

The schematic for the comparator is shown in Figure 5. The comparator uses the same differential pair as the op-amp for an input stage, followed by a high gain common source output stage. After amplifying the input signal the digital output is latched by a simple master-slave D flip-flop. The comparator uses 40μA of DC current and consumes 36μW. The output of the comparator settles to its final value within 10ns of the latch closing.

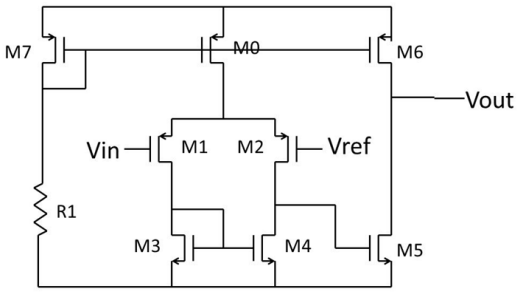

Figure 5: Comparator schematic.

3 PHYSICAL IMPLEMENTATION AND MEASUREMENT RESULTS

Overall simulation results for the modulator are shown in Table 1 while the power spectrum density plot is shown in Figure 6. This plot shows regular noise spikes at the 3rd harmonic and above of the input tone which are easily filtered out by the low-pass filter characteristics of the decimation filter. The modulator achieves a SNDR of 61.2dB resulting in a 10 bit effective resolution while consuming 165μW.

Table 1: Modulator performance.

Parameter	Results
SNDR	61.2dB
Effective Number of Bits	10
Power Consumption	165μW

The physical layout of the modulator covers an area of 0.0225mm^2. Many measures were taken to ensure that transistor mismatch and signal distortion were minimized throughout the layout. All matched transistors in the op-amps and comparator were implemented using common centroid layout techniques, and all analog transistor blocks are surrounded by guard rings. The 4 phase, non-overlapping clock generation circuit is also isolated via a guard ring. Finally, wires carrying important digital and analog signals throughout the chip are isolated with grounded lines to minimize interference and crosstalk.

The proposed modulator was fabricated and its functionality verified on silicon. An oscilloscope screen capture in Figure 7 shows the modulator performing as expected with a 1 kHz sine wave input. A die photo of the test chip is shown in Figure 8.

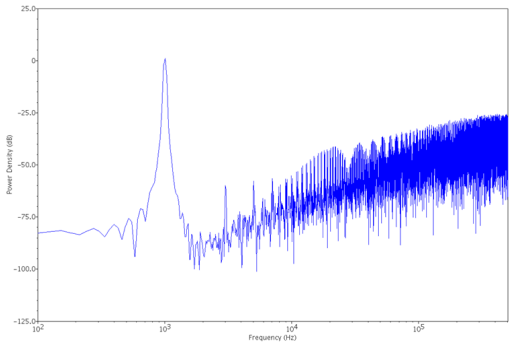

Figure 6: Modulator output spectrum.

4 CONCLUSIONS

A low power, second order, Sigma-Delta modulator for use in an integrated biosensor system was presented in this paper. The proposed modulator uses a 900mV supply voltage to reduce power consumption and extend the life of battery powered biosensors. The modulator achieves a signal-to-noise distortion ratio of 61.2dB and consumes 165μW. Compared

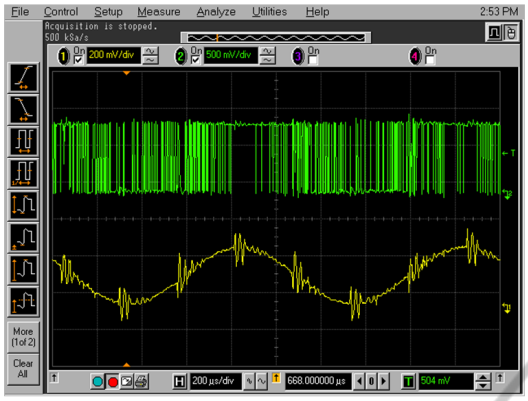

Figure 7: Silicon test results.

to existing low-power designs the proposed modulator performs very well balancing SNDR and power consumption. Table 2 compares the performance of the proposed modulator against existing designs.

Table 2: Performance comparison.

Design	SNDR	Proposed Auto-zeroed
(Lei, 2010)	68.85dB	800μW
(Jasutkar, 2011)	68dB	400μW*
(Goes, 2006)	80.1dB	200μW
(Lee, 2006)	50dB	180μW
This Work	**61.2dB**	**165μW**

*(Jasutkar, 2011) quoted power consumption as 400W, corrected to 400μW here.

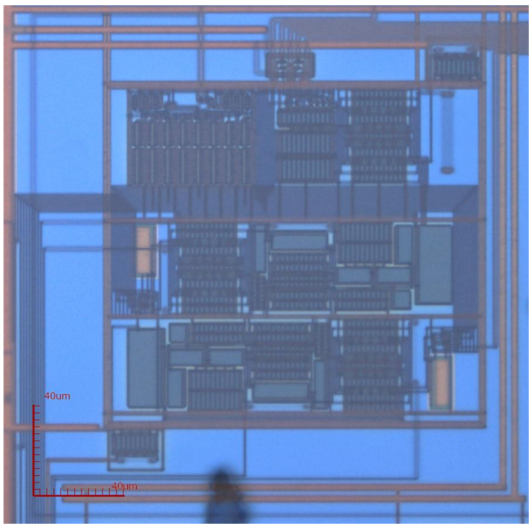

Figure 8: Die photo.

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