Wireless Energy and Data Transmission ASIC for Blood Pressure Measurement in an Aneurysm Implant

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Abstract: Aneurysm implant requires multiple pressure sensors integrated into the stent graft for recording pressure profile inside an aneurysm sac. This paper details the design of an ASIC which receives power wirelessly using inductive coupling, fetches pressure data from a seperate chip and transmits data wirelessly. Besides, the ASIC extends the functionality of the external pressure measurement chip to support up to four pressure sensors by using an analog multiplexer. Error detection and forward error correction are implemented to improve data integrity for wireless data transmission. The design has been implemented and tested in 350 nm CMOS technology.

1 INTRODUCTION

Aneurysm is the dilation of the artery due to weakening of the arterial wall, which occurs in 5-10% of older men and in 1-2% of older women (Silverstein et al., 2005). Endovascular aneurysm repair (EVAR) using an implantable stent graft is a minimally invasive method for abdominal aortic aneurysm treatment. The complication after an EVAR stent insertion is the endoleakage, which is the leakage of blood around the stent graft (Drury et al., 2005).

Endoleak will add trauma to the weakened arterial walls of the aneurysm, which can cause further enlargement or even risk of rupture. Most of the endoleaks are discovered within 30 days of operation but sometimes they do not manifest themselves until up to 7 years after surgery (Corriere et al., 2004). Up to 40% of patients underwent EVAR suffer from endoleak. The long time window of the endoleaks and high probability of its occurrence necessitates monitoring of the patients periodically for many years.

Currently, contrast-enhanced computed tomography (CT) or ultrasound is used to detect endoleaks after EVAR operation. This method does not allow real-time measurement of intrasac aneurysm pressure level, and it require patients to visit hospital periodically. These shortcomings can be reduced by using a new approach. This approach integrates pressure sensors into the commercially available stent graft used for EVAR repair. Pressure sensors together with other electronic components form an implant. This implant must transmit pressure data wirelessly and it should be powered wirelessly (Koops et al., 2013).

2 IMPLANT REQUIREMENTS

The implant consists of an array of pressure sensors evenly distributed and mounted on the outer surface of the stent graft for assessing pressure distribution in the aneurysm sac with high spatial resolution. The pressure data is sent wirelessly and the implant is powered wirelessly by inductive coupling. The implant together with stent graft must be able to fit into a commercially available 24F applicator stent delivery system (Spink et al., 2015).

The implant is located inside the body of the patient where the distance between the wireless power sender and the implant is greater than 10 cm. So the sensors and electronic components in the implant must work at very low-power. The implant should survive mechanical stresses generated due to the stent insertion procedure during EVAR operation. For a good mechanical performance, it is advised to have few electronic components integrated on a flexible PCB substrate to be mounted on the stent (Bradford

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et al., 2010).

This ASIC design aims to minimize the number of electronic components in the implant to be mounted on the stent. This is realized by integrating wireless power reception and wireless data transmission on a single die. Furthermore, instead of state of the art resistive sensors, a capacitive pressure sensor is used in order to reduce power consumption. An external(off-chip,on stent) Capacitance to Digital Converter (CDC) chip, ZSSC3123 (ZMDI, 2015), is used to drive the capacitive pressure sensor. The die of ZSSC3122 is used to fit into the dimension of implant. The CDC can support only one pressure sensor, but the ASIC extends this functionality to support up to four sensors using an analog multiplexer designed on chip. Further the CDC can be designed on-chip for independent solution.

3 ARCHITECTURE AND DESIGN

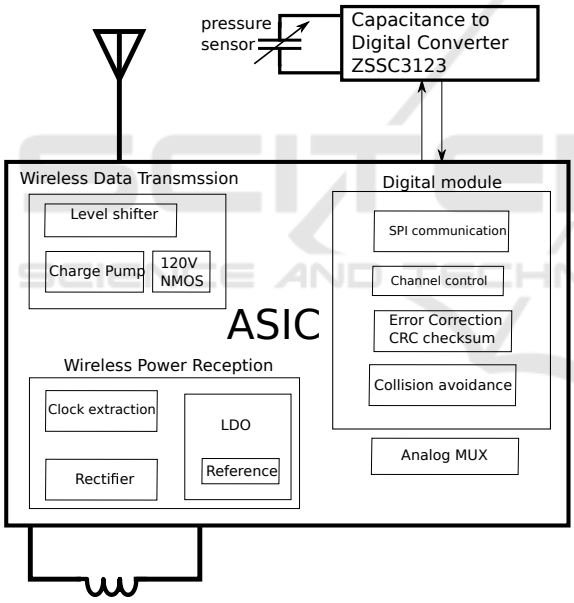

Figure 1: Chip architecture.

A block diagram of the ASIC is shown in figure 1. It consists of three main modules: wireless power reception, wireless data transmission and the digital module. The wireless power reception module receives energy through inductive coupling to power the whole implant. It has on-chip rectifier and Low Dropout Regulator(LDO) which converts sine signal into regulated 3.3V supply for full chip. An on-chip digital module fetches the pressure sensor data from the CDC chip and sends it to the wireless data transmission module. The wireless data transmission module transmits the pressure data to the outside world.

3.1 Wireless Power Reception

The wireless power receiving module provides a regulated constant output voltage of 3.3 V from the wireless energy received from the resonant LC circuit. The block diagram of this module is shown in figure 2. An off-chip resonance circuit consisting of L and C1 receives wireless power through inductive coupling. The output of the resonace circuit is connected to the chip's input as depicted in figure 2.

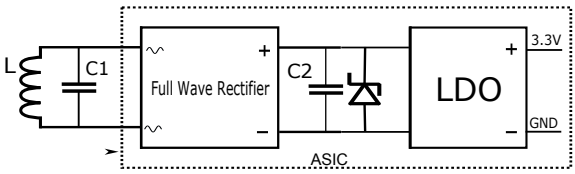

Figure 2: Wireless power reception module.

The Capacitor C2 is used for energy storage and the zener diode for overvoltage protection.LDO has been used to provide a stable DC supply voltage of 3.3V and power of 1mW to the rest of the modules in the ASIC.

3.1.1 Rectifier

The rectifier is the first front end block of the ASIC which converts the wirelessly received AC signal into pulsating DC signal. There are fundamentally two types of rectifiers, half wave and full wave rectifier. In this ASIC a full wave rectifier has been designed because of it's high efficiency. The conventional full wave rectifier has the fundamental problem of threshold drop at the output. The cross coupled structure has been used for this threshold cancellation (Kotani et al., 2009) (Kotani and Ito, 2007) as shown in figure 3. In spite of the threshold voltage (Vth) cancellation, the rectifier suffers from uncontrolled biasing of the mosfet rectifier diodes (Kotani et al., 2009) which leads to high leakage current as shown in figure 4. During the turning on of MP2 and turning off of MN2, there is an intermediate state when both MP2 and MN2 conduct as seen in figures 3 and 4. This causes current flow from DC_output to ground as leakage current. This paper proposes a modified design which uses a cross coupled capacitive divider-based static biasing of the NMOS diodes (MN1 and MN2) to reduce the mentioned leakage current and obtain high efficiency.

In the conventional design shown in figure 3, for the positive half cycle MP2 and MN1 conduct whereas for the negative half cycle MP1 and MN2 conduct (Kotani and Ito, 2007) (Kotani et al., 2009). During the time when the sine input signal changes from low to high or high to low, there is a leakage

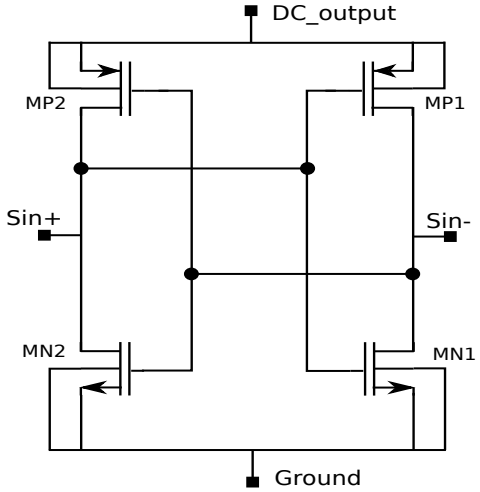

Figure 3: Conventional rectifier with Vth cancellation.

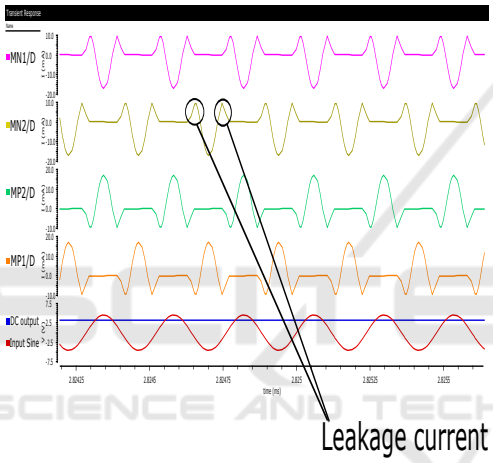

Figure 4: Conventional rectifier output.

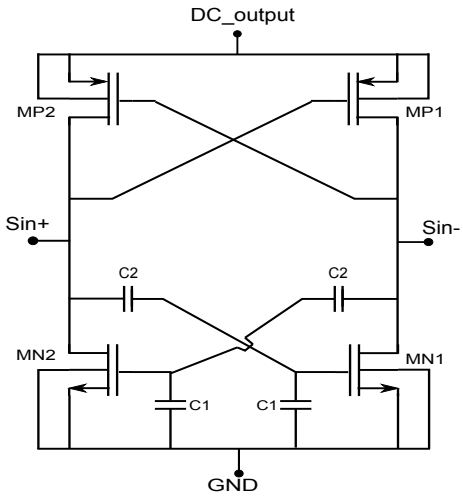

Figure 5: Rectifier circuit of the ASIC.

current which is labelled as ”Leakage current” in the figure 4. In the proposed rectifier design shown in figure 5, a static biasing has been done for MN1 and MN2 which allows MN1 and MN2 to conduct only for the time when MP2 and MP1 conducts, providing an extremely low leakage shown in figure 6 and high efficiency of 74%. The capacitive divider C1 and C2 divides the voltage level between Sin+/Sin- and ground. The ratio of C1 and C2 is selected so that the voltage at the gate reaches Vth only when the input sinus voltage is above DC output voltage.

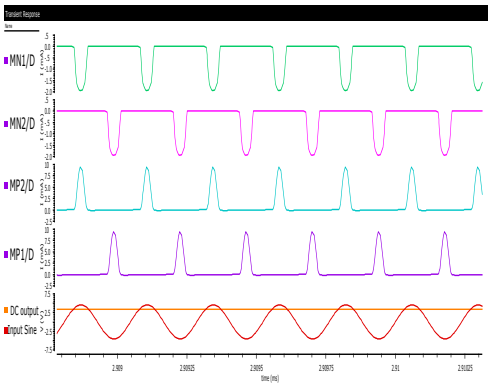

Figure 6: Rectifier output of the ASIC.

3.1.2 Low Dropout Regulator

The conventional low dropout regulator (Milliken et al., 2007) has been designed in this ASIC with resistive feedback as shown in figure 7.

$$Vout = (1 + \frac{R1}{R2}) \times Vref$$

where Vref is the referance voltage generated by the on-chip bandgap.

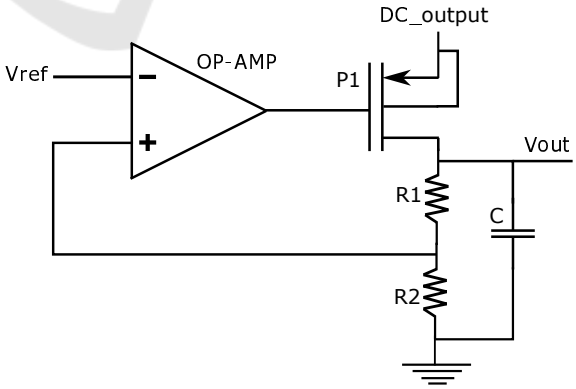

Figure 7: Low Dropout Regulator.

The regulation of the output voltage starts when the rectifier input voltage is above 9V (peak to peak) and DC_output above 3.3V. Figure 8 shows the comparison between simulated and measured output voltage of the LDO for different rectifier input voltages.

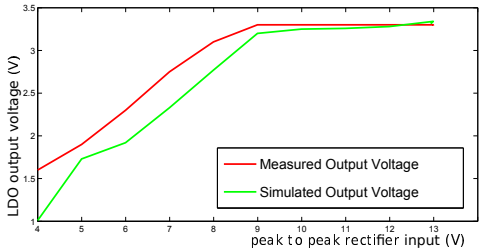

Figure 8: Measured and simulated output voltage of the wireless power receiving block.

3.2 Digital Module

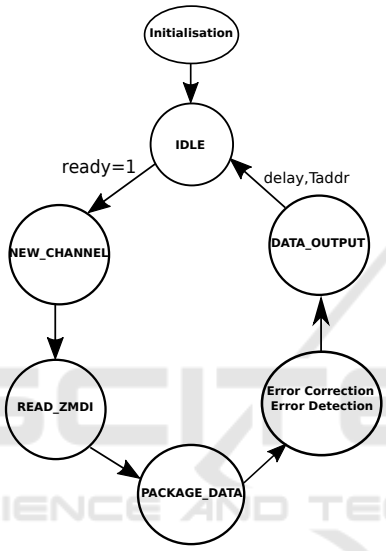

Figure 9: Finite state machine.

The clock extraction block (figure 1) provides clock input for the digital module. The frequency of this clock is dependent on the frequency of the external (outside body) wireless power sender. An internal clock divider in the digital module reduces this frequency down to 3 kHz. This has been done to reduce the power consumed by the digital module.

The Commercially available CDC supports only one pressure sensor. The on-chip analog MUX multiplexes the excitation signal generated by the CDC to one of the four pressure sensors based on the input channel settings of the digital module.

The digital module is implemented using the Finite State Machine (FSM) as shown in figure 9. This module communicates with the CDC using an SPI interface. The 'Ready' signal is an interrupt from the CDC signalling new pressure data. After reception of 14 bit pressure value, a new channel is selected to switch CDC excitation signal to a new pressure sensor. Later, pressure data is fetched from the CDC.

An error in the received data at the external (outside body) reader hardware is identified using a Cycle Redundancy Checksum (CRC). The polynomial used for this CRC is $p(x) = x^5 + x^2 + 1$.

In a traditional approach, when corrupt data is identified by the external reader hardware, it either discards the whole data packet or signals the implant to resend the data. Resending data approach costs further area for wireless data reception (envelope detector, amplifier, comparator etc...) on the chip and extra energy for data re-transmission. This can be avoided by using Forward Error Correction (FEC).

Reed-Solomon error correction is implemented in this chip (Tej and Jhansi Rani, 2013). By adding 16 bits of Reed-Solomon code to the 20-bits of data, it is possible to correct up to 8-bits of data. The parameters of the Reed-Solomon code are m=4, n=9, k=5 and t=2. The generator polynomial $g(x) = x^4 + 13x^3 + 12x^2 + 8x + 7$ is based on the primitive polynomial $p(x) = x^4 + x + 1$.

START (4 bits)	Address, pressure value, channel (20bits)	Error Correction (16 bits)	CRC-5 (5 bits)	STOP (1 bit)
1111	addr0, addr1, C0, C1....C12, C13, ch0,ch1,addr0,addr1	EC0,EC1,....,EC15	crc0,..crc4	1

Figure 10: Data packet output of the digital module.

The data packet is shown in figure 10. The data containing address of the chip, pressure value and the channel number counts to 18 bits. But two address bits are added again to it make it 20 bits (k=5) because error correction is performed on a block of 4 bits (m=4). To identify multiple ASIC's on the stent graft, each ASIC is assigned with a unique address. Two address pins are used for this purpose. The clock frequency of the digital module is dependent on this address inputs. Figure 11 shows the clock of the digital module and the pulsed data packet output for wireless data transmission. Data output of the digital module are pulses having a duty cycle less than 0.1 % and pulse width of 1 μs. This pulse width is choosen based on the estimated time constant for charging the inductor in the wireless data transmission module.

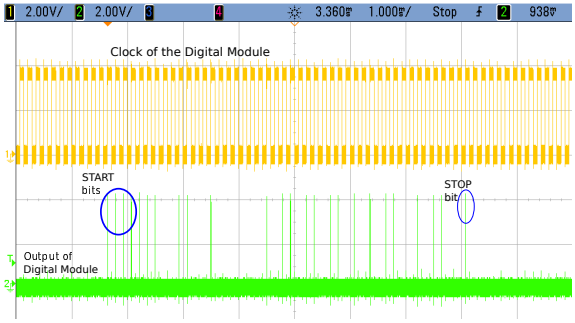

Figure 11: Measurement results of the digital module.

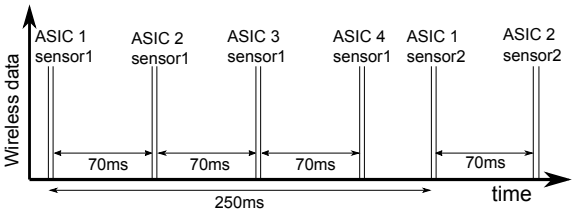

Figure 12: Time division multiplexing for wireless data transmission.

Up to four ASIC's can be mounted on a single stent. All ASIC's are powered by a single external(outside body) wireless power sender. Since they are powered simultaneously, data collision might occur. This can be avoided by utilizing time division multiplexing as shown in figure 12. Since there is only one data packet every 250 ms, each ASIC transmits data on a specific time slot. This time slot is decided by the address of the ASIC and it is shown as a delay (Taddr) in the FSM. The delays are 0 ms, 70 ms, 140 ms, 210 ms for address input of 0 to 3.

The pulse duration of the bits in the data packet of the digital module also depends on its address. It varies from 0.33 ms, 0.25 ms, 0.2 ms and 0.14 ms based on the address of the ASIC (from 0 to 3).

3.3 Wireless Data Transmission

The wireless data transmission module transmits the data packet received from the digital module to the external(outside body) receiver. New data packet is available every 250 ms and it takes about 15 ms for wireless data transmission. The ASIC is designed to transmit 4 data packets per second, each packet containing one of the four pressure sensor's recorded data.

During idle time of the data transmission module, the energy needed for the data transmission is stored on a capacitor using a charge pump. This stored energy is then used to send pulses corresponding to the data bits.

3.3.1 Charge Pump

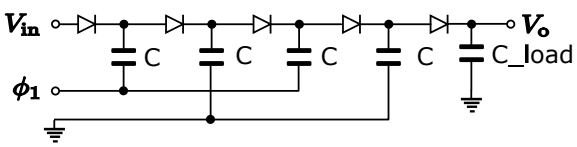

Figure 13: Dickson charge pump.

A Dickson charge pump has been designed for energy storage in an off-chip 1 uF capacitor, C_load (Dickson, 1976).The high capacitance has been used to store higher charge which is used to charge the inductor L1 with high current. The charge pump charges the load capacitor generating an output voltage of 20 V. The total time taken to reach the needed charge is about 225 ms. An oscillator is used to generate a clock with 50% duty cycle. Single clock was used instead of a non-overlapping clock cycle in order to reduce the total power consumption of the charge pump module as shown in figure 13.

The capacitor values for each stage of the charge pump were chosen based on the available chip area and the output power requirement for wireless data transmission.

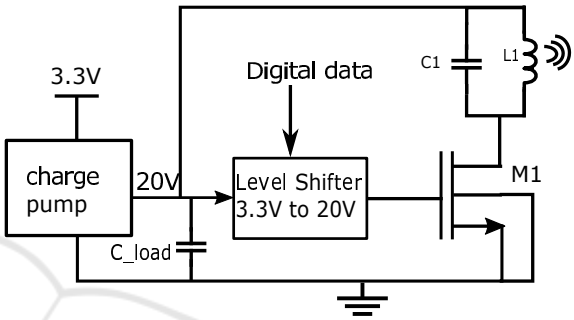

Figure 14: Wireless data transmission.

3.3.2 Data Transmission

A block diagram of the wireless data transmission module is shown in figure 14. A level shifter shifts the voltage level of the digital data from 3.3 V to 20 V in order to drive the transistor. The 120V NMOS output transistor M1 is connected to an off-chip resonance circuit load (L1 and C1). When the digital data is HIGH, then NMOS is turned on and the inductor L1 starts storing energy. When M1 switches off the inductor discharges through C1 generating a magnetic field and a high voltage spike at the drain of M1. 120V NMOS device has been choosen from H35B4D3 AMS process to sustain this high voltage. This magnetic field is detected by the external reader hardware. The frequency of the data transmission is dependent on the values of L1 and C1. The external hardware uses a resonant circuit tuned to the data transmission frequency.

At each pulse, when M1 turns off a high drain-source voltage spike is created by the L1 inductor due to the stored energy in the inductor as shown in figure 15. The slow decrease in the voltage level of the pulses is due to discharge of the storage capacitor (C_load) with each bit of transmission.

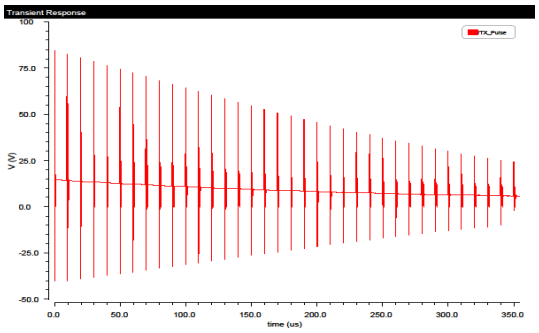

Figure 15: Drain-source voltage (Vds) of the M1 transistor.

4 CONCLUSIONS

An ASIC for wireless energy harvesting and wireless data transmission for blood pressure measurement is presented in this paper. The ASIC was fabricated using 350 nm high voltage CMOS technology. The fabricated chip is shown in figure 16. The chip has an area of 2.3 mm x 1.3 mm and consumes approximately 1 mW. The small dimension and low power consumption of the chip makes it suitable for implantable application. The chip is tested for wireless power reception at a frequency of 4 MHz. Clock extraction from the wireless power is used for the digital module and the communication between the chip and the CDC.

Forward error correction was implemented to improve data integrity and to save area on the chip by avoiding extra circuitry for wireless data reception. The analog muliplexer extends the functionality of the CDC chip to support four pressure sensors instead of one.

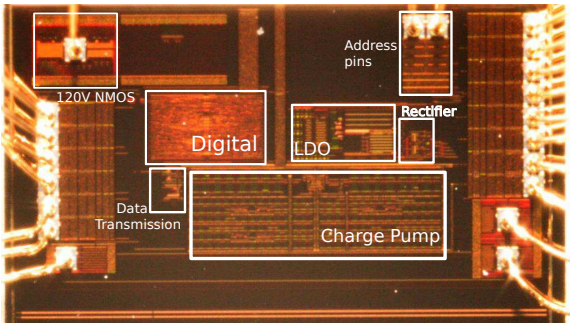

Figure 16: Fabricated ASIC (2.3mm x 1.3mm).

The chip has been tested and development of a wireless blood pressure sensing implant is in progress for EVAR and in-vivo test.

ACKNOWLEDGEMENTS

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