A Self-duty-cycled Digital Baseband for Energy-enhanced Wake-up Receivers

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Abstract: An ultra low-power digital baseband (DBB) for Wake-up Receiver (WuRx) is presented. Based on low power microcontroller (MCU), the DBB power gates the WuRx peripherals to further reduce their average energy consumption. It issues low duty-cycling signals with very short power-on periods, allowing very low latency between a transmitted WuPt and its detection. The latency and power consumption tradeoff can be adjusted to meet different application requirements. The presented circuit implements low-power listening protocol as a duty-cycle scheme and also emphasizes the possibility to decode more than 512-bit address pattern.

1 INTRODUCTION

A battery is an exhausting energy resource used by wide range of devices. WSN feeds off batteries, thus conserving energy is essential. Replacing or changing batteries in WSN can be costly and difficult to realize. In practical cases, the lifetime of a WSN reaches its end when all devices (wireless sensor nodes) within the network go permanently inaccessible. A depleted battery can be one of the causes. Radio chip, in a wireless node, consumes the most energy with reference to the rest of node's components (i.e., sensors, microcontroller (MCU)). The radio's permanent activity is often not necessary in WSN. Therefore, switching it to sleep state can drastically preserve energy. To prevent a sensor node from being totally disconnected from the network during the conventional radio's sleep period, a much lower power radio receiver can be used instead. The latter is referred to as (WuRx). Generally, its main purpose is to continuously listen for an incoming wake-up packet (WuPt). It is communicated from a different node. Upon WuPt reception, the WuRx, then, issues an interrupt to the MCU, which, in return, wakes-up the main transceiver. WuRx should be based on simple architectures to keep the overall complexity of a sensor node to a minimum. Other characteristics are sensitivity, data rate and energy usage. In a WSN where each sensor node is embedded with a WuRx, the latter should distinguish between different WuPt. This is done by including a unique destination address in every WuPt. The DBB deals with the address pattern correlation and issues a logic signal if it is addressed. This way, unnecessary MCU active/sleep toggling is avoided and more energy is saved.

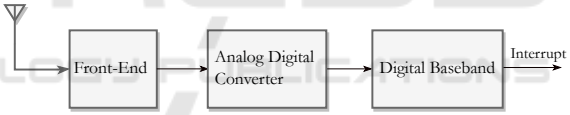

Figure 1: Simplified typical WuRx block diagram.

Depending on how dense is the WSN, the WuPt includes a unique pattern for every node, coded in 16, 32, 64 bits, etc. On-off keying (OOK) is often used for modulation schemes as it allows low-complex architectures. However, this can impact the overall sensitivity and power demand of a WuRx. Several DBBs are introduced in recent works to optimize the mentioned features. (Bdiri and Derbel, 2015)(Gamm et al., 2014) use AS3932 (Austrian Mikro Systeme, 2015a) or AS3933 (Austrian Mikro Systeme, 2015b) as an off-the-shelf DBB. The chip eliminates the need of a digitizer (i.e, comparator), meaning that it is able to condition an analog representation of the pattern bit sequence. The minimum sensitivity reaches down to 80 μV_{RMS}. The chip consumes more than 5 µW when listening and 24 µW during pattern decoding. The authors in (Magno et al., 2016) used an MCU to deal with the decoding mechanism. With no RF activity, the MCU is at its lowest sleep state consuming 40 nW. It activates the core at 8 MHz upon reception of the WuPt preamble, followed by WuPt correlation, dur-

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ing which, it drains 300 µW. This indicates that the more WuPt the WuRx receives the more it consumes.

In (Mazloum et al., 2016), another design based on flip-flops is introduced. The DBB is optimized for a specific duty-cycled WuRx, specifically DCW-MAC (Mazloum and Edfors, 2011). At 250 kbit s^{-1}, it consumes 0.9 µW. A complex programmable logic device (CPLD) and a field-programmable gate array (FPGA) can be used to act as DBB for WuRx. The energy consumption, however, is still higher than most of the introduced DBB (Petäjäjärvi et al., 2016)(Jean-François et al., 2013). In this work, a DBB for duty-cycled WuRx is introduced. The detection procedure is based on low-power listening (LPL) protocol (Polastre et al., 2004). It is safe to say that the DBB is fully flexible to implement different MAC protocols depending on the application prerequisites. The introduced DBB offers scalability in terms of address pattern length, data rate and energy consumption. This paper is organized as follows: In section II, details and analysis of the design process are discussed. Section III reports the measurements done on a fabricated WuRx with the presented DBB. Finally, section IV concludes the proposed work.

2 SYSTEM DESCRIPTION

The proposed solution relies on maximizing WuRx's sleep time instead of constantly monitoring the channel. It allows the adjustment of several parameters such as destination address length, data rate and WuPt detection latency. This flexibility makes the WuRx suitable for a wide range of applications. A low-power MCU PIC12LF1572 (Microchip, 2015) is used to design the back-end of WuRx. The MCU periodically wakes-up then enables the rest of WuRx components. If any RF signal is fed through the front-end during this brief time duration T_{ON}, the MCU waits for a corresponding WuPt preamble. If it is the case, it keeps the active components active to receive the rest of WuPt. A decision is made depending on the correlation results followed by switching off all active components. The MCU switches to sleep state for T_{S} until the next wake-up period. The MCU waits for preamble detection during T_{ON}. The power dynamically increases proportionally with the number of successful preamble detections.

In the case where there is no WuPt, all components are turned off and the MCU turns back to sleep. Fig. 2 illustrates the timing diagram where the MCU successfully detects/misses a WuPt. The illustrated arrival time of the WuPt is considered the best case scenario as the MCU activates for the minimum necessary time T_d. The opposite case is when the preamble is detected at the very beginning of the WuPt. Then, the MCU has to process the entire WuPt, wasting more energy. Let β be the mean interval between two transmitted WuPts. The DBB's average power consumption is calculated as follows:

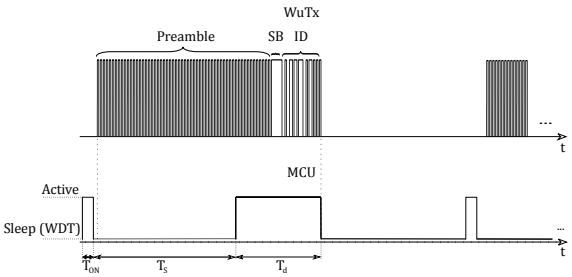

Figure 2: Simplified timing diagram of WuPt and duty-cycled MCU in channel listening.

$$P_{avg} = \frac{P_{\mathrm{ON}}(\beta T_{\mathrm{ON}} + T_{\mathrm{S}}(T_d - T_{\mathrm{ON}})) + P_{\mathrm{WDT}} T_{\mathrm{S}}(\beta + T_{\mathrm{ON}} - T_d)}{\beta(T_{\mathrm{ON}} + T_{\mathrm{S}})} \quad (1)$$

where P_{ON} and P_{WDT} are the power consumption of the MCU at active state and sleep with watchdog enabled, respectively. The detection is performed in a purely asynchronous scheme. OOk is employed for a low-power front-end architecture.

2.1 WuPt Structure

The WuPt contains a preamble, separation bits (SB) and destination address pattern (ID). The preamble $\{p_0 \dots p_{i-1},\ i \in \mathrm{N}\}$, consisting of i-bit, helps the MCU detect the presence of WuPt. SB $\{s_0 \dots s_{j-1},\ j \in \mathrm{N}\}$ are composed of j-bit. The sequence separates preamble and the ID.

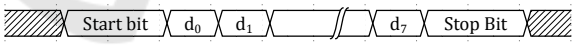

Figure 3: 8-bit ID sequence diagram.

Let $k \in \mathrm{N}$. The ID consists of k times 10-bit sequence where $\{d_0 \dots d_7\}$ are the 8-bit ID and 2 bits for a start and stop bits. $k = 2$ and $k = 4$ represent 16-bit and 32-bit IDs, respectively. Depending on the memory of the MCU, the latter can decode more than 512-bit. The start and the stop bits help the MCU localize the pattern.

2.2 Back-end Architecture

Instead of continuously waiting for an incoming WuPt, the self-duty cycled MCU wakes-up periodically to monitor the channel. When the MCU enters sleep state, all its internal peripherals are automatically disabled except for the watchdog timer (WDT). By enabling the latter, the MCU can toggle between

active/sleep state without the need for an external timer. The more interesting characteristic of the WDT lies in its energy consumption with only 260 nA at 1.8 V. When WDT overflows, the MCU is interrupted and switches to active state. The WDT's time-out represents also the sleep period t_S of the WuRx. This can be configured between 1 ms and 256 s (Microchip, 2015). When the MCU enables all active elements of the WuRx, it holds waiting for a WuPt preamble (i.e., '010101...') till an elapsed duration of T_{ON}. Upon the reception of the preamble, the MCU counts the positive edges of each single p_{i-1} bit for i_c times. The counting stops if it reaches n ($i_c = n$), where n is a user-defined number of positive edges the MCU has to detect. If $i_c < n$, the detection is considered erroneous, then the MCU turns-off all external peripherals and switches back to sleep.

Any interfering signal, that has a baseband frequency higher or lower than f_c, is rejected by the MCU by means of digital filtering. This is done by continuously polls an input pin for a certain period of time t_p, in a way that if the positive edge comes sooner or later than expected the preamble is rejected. Let f_c be the modulated signal frequency. The choice t_p is done by the following equation.

$$\frac{1}{f_c} < t_p < \frac{2}{f_c} \tag{2}$$

The choice of T_{ON} depends on t_p and the power-on time t_{POWER} of all peripherals including the MCU. The minimum T_{ON} should obey the Eq. 3.

$$t_{POWER} + t_p < T_{ON} \tag{3}$$

In the different case of successful preamble detection, the MCU remains active and waits for s_{j-1}-bit. The SB structure is a successive j of '1' bits. If SB sequence is received, the MCU enables the enhanced universal synchronous asynchronous receiver transmitter (EUSART). The latter is a peripheral within the MCU dedicated for serial communication. The usage of EUSART excludes the need of a software implementation for serial data reception. The correlation process starts upon reception of the first '0' bit (start bit) after SB. The EUSART stores the $\{d_0 \dots d_7\}$ in a byte register to be read later on. The process is repeated k times until the processing of all ID frame takes place. The MCU, then, compares the received byte(s) to the stored value(s). The comparison brings the decision to either issue an interrupt or not to an external unit. In the end, the MCU disables the EUSART and all WuRx's peripherals. The decoding process takes time T_d and affects dynamically the average power consumption of DBB. In the following section, we configure the MCU with the required parameters to evaluate its performance.

3 SYSTEM EVALUATION

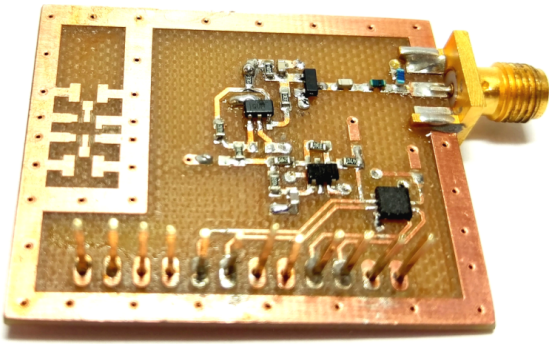

Figure 4: Assembled wake-up receiver with the presented DBB on 1.55 mm thick printed circuit board (PCB).

The front-end published in (Bdiri et al., 2016) is used to implement and evaluate the DBB. It consists of an envelope detector that performs an RF to DC conversion. Then an amplifier boosts the signal an forward it to an analog to digital convertor. In the end, the logic signal is fed to the DBB. Only the electrical characteristics of the MCU are taken into account for the final measurements. Fig. 4 shows all the assembled components on a PCB. T_S represents the latency of WuPt detection since at that time the DBB is at sleep state. It is configured by acting on the watchdog timer. For the sake of the complete system evaluation, the DBB it is set to perform preamble detection every $T_S = 32$ ms. Moreover, when exiting sleep mode, the high frequency internal oscillator (HFINTOSC) is activated, which requires a certain time to stabilize. For the PIC12LF1572, the HFINTOSC warm-up time $t_{POWER} = 5\,\mu$s. 16 MHz is chosen for the core frequency to allow maximum processing speed at which, the MCU demands a power $P_{ON} = 1$ mW. 32 MHz requires a phase locked loop (PLL) and needs more than 2 ms to settle. The WuPt modulated frequency is chosen $f_c = 128$ kHz. From Eq. 2, t_p is calculated $t_p = 8\,\mu$s. Hence, from Eq. 3, $T_{ON} = 13\,\mu$s. Using these parameters on the Eq. 1, P_{av} can be simulated against the mean average interval β for minimum and maximum durations of T_d. The latter depends on the WuPt arrival time and when it coincides with the MCU's preamble polling. Fig. 5 shows the obtained results. For $\beta > 1000$ s the average power is $P_{av} < 0.9\,\mu$W for $T_S = 32$ ms.

The MCU is configured to correlate a 24-bit ID $\{$`0x55`, `0x69`, `0x96`$\}$. Fig. 6 shows a successful decoding process finished by issuing a pulse at an output pin.

The duty-cycle obeys the LPL protocol. This can cause overhearing issues in a dense WSN, thus increasing energy consumption. The DBB allows flexible implementation of different MAC protocols as to

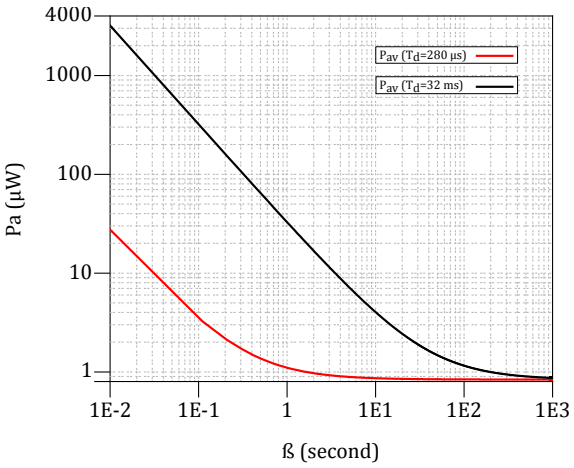

Figure 5: The MCU's average power consumption against the mean interval time β for different decoding durations T_d.

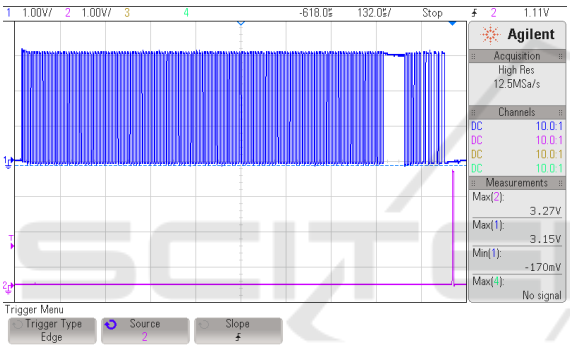

Figure 6: Oscilloscope screen capture of a correlated WuPt's ID (blue). A generated pulse (pink) indicates a matching ID with the register values

address specific applications demands.

4 CONCLUSION

An MCU-based back-end for duty-cycled wake-up receivers is introduced. It operates as a DBB with addressing capabilities and also controls the activity of WuRx peripherals to reduce the overall energy consumption. The MCU is fully configurable either by an external unit or by acting on its firmware. Main configuration parameters including latency, data rate and ID length allow a wide range of input values. A prototype is realized as to evaluate the the intended features. For a latency of $T_S = 32$ ms, the DBB consumes less than 1 µW. The power consumption depends on timing parameters, which can be configured depending on the application requirements. Additionally, several MAC protocols can be implemented to improve different performance measures, including energy consumption, overhearing issues and latency.

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