A Sub-1V Bandgap Voltage Reference with Improved PSRR Scheme

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Keywords: Bandgap reference, power supply rejection ratio, temperature coefficient, error amplifier.

Abstract: A High performance sub-1V bandgap voltage reference (BGVR) with high power supply rejection ratio (PSRR) and low temperature coefficient (TC) is proposed in this paper. An improved PSRR scheme is inserted to isolate the supply voltage of the error amplifier and the supply voltage of BGVR core from a power supply source in order to achieve a high PSRR. The proposed circuit is designed and simulated in 0.18µm CMOS 1.8V/3.3V technology. The proposed BGVR deliver an output voltage of 0.6346V at 27°C and the measurement temperature coefficient is 22,3ppm/°C over temperature range -40°C to 140°C, the DC value of PSRR is -93dB at 10kHz and -71dB of PSRR is achieved at 1MHz and a line regulation of 104µV/V is achieve over supply voltage range 1.2V to 1.8V. The area of layout is 0.0337 mm^2. The proposed sub-1V bandgap voltage reference is suitable for low power LDO regulators and switching regulators.

1 INTRODUCTION

Bandgap voltage reference is a circuit used to generate a fixed voltage, V_{REF}, that in theory is independent of the power supply voltage V_{DD} (where $V_{REF}<V_{DD}$), temperature, and process variations. In other words, the ideal reference voltage is independent of PVT. Voltage reference is among the most important subcircuit in analog integrated circuits and is used as an internal voltage reference in linear regulator (LDO), switching regulator, analog-to-digital converter (ADC) and digital-to-analog converter (DAC) and other analog integrated circuits. This is achieved by adding a voltage, which is proportional to the absolute temperature (PTAT), to a base-emitter voltage of diode connected Bipolar Junction Transistor (BJT) NPN or PNP type which is a complementary to the absolute temperature (CTAT) in order to compensate for its first-order temperature dependency (Razavi, 2017).

The classical design of BGVR circuits commonly has an output voltage V_{REF} around 1.25V (close to the theoretical 1.206V bandgap voltage of silicon at 0 K) (Widlar, 1971; Kujik, 1973; Brokaw, 1974; Tzanateas et al., 1979; Song and Gray, 1983).

As the technology scales less than 350 nanometers, so do to supply voltages. The supply voltages recently tend to be in the range of 0.6-1.2V. The supply voltage scales with the technology, but the threshold voltage of the transistors does not scale at the same rate. This makes it difficult to incorporate conventional design of bandgap voltage reference to operates properly in the low supply voltages. For the low voltage bandgap reference design many approaches have been proposed; resistive divider networks (Banba et al., 1999; Leung and Mok, 2002; Ker et al., 2006), Current summing and a voltage summing circuits (Ripamonti et al., 1999), transimpedance amplifier (Jiang and Lee, 2000), dynamic threshold mosfets (Annema, 1999). Other circuits have been proposed for the design of sub-1V BGVR to have a low temperature coefficient and at the same time a high PSRR (Andreou et al., 2012; Xin et al., 2009), but they have always limited by the short channel effects existing in nanometer technologies which has a very low supply voltage, and especially in the design of the opamp with very low input offset voltage which remains an important element in the BGVR circuit to provide a precise voltage (or current) proportional to the absolute temperature V_{PTAT} (or I_{PTAT}) because a very low offset guarantees the obtaining of this voltage (or this current).

This work propose a novel design for sub-1V bandgap voltage reference generator while provide an output voltage reference V_{REF} with low TC and high PSRR and good line regulation. In section 2,

Slamti, A. and Lakhliai, Z.
A Sub-1V Bandgap Voltage Reference with Improved PSRR Scheme.
DOI: 10.5220/0009772701850193
In *Proceedings of the 1st International Conference of Computer Science and Renewable Energies (ICCSRE 2018)*, pages 185-193
ISBN: 978-989-758-431-2

the conventional scheme of the sub-1V bandgap voltage reference is analyzed to show the limits of its performance. In section 3 a related work of high PSRR structure of bandgap voltage reference is presented. In section 4, the scheme of the proposed circuit is given and a detailed analysis of BGVR core generator is presented and the literal expression of the output voltage reference is established in order to show the design method of this block, also the small high frequency signal model of the proposed circuit is presented in order to calculate the lateral expression of the PSRR. In section 5, the simulation results are given to show the performance of the proposed circuits and a comparison with related works is presented. Finally in section 6 a conclusion is given to show the contribution of the proposed circuit.

2 CONVENTIONAL SUB-1V BANDGAP VOLTAGE REFERENCE

The conventional sub-1V bandgap voltage reference suitable for low power supply is shown in Figure 1 (Banba et al., 1999). He use an opamp based β-multiplier architecture with resistive division, where an opamp works as an error amplifier will form an inverted feedback loop to enforce the two input nodes X and Y of the opamp having the same voltages.

The current mirror is formed by the PMOS transistors M_1, M_2 and M_3 having identical size, such that the currents flowing through this three transistors are the same. The β-multiplier consists of two diode connected NPN transistors Q_1 and Q_2, with their emitter area ration being 1:K to provide the required temperature dependent voltages to construct the voltage reference circuit.

The output voltage reference V_{REF} is expressed as:

$$V_{REF} = \frac{R_3}{R_2}.(V_{BE_1} + \frac{R_2}{R_1}.\ln K.V_T + \frac{R_2}{R_1}V_{OS}) \quad (1)$$

Where, V_{BE_1} is the base-emitter voltage of BJT Q_1 witch it's had a negative temperature coefficient and represents the CTAT voltage.

And V_T is the thermal voltage (V_T=25,9mV at 300K) expressed as,

$$V_T = \frac{k_B.T}{q} \quad (2)$$

Where k_B is the Boltzmann's Constant (k_B=1,381.10^{-23}J.K^{-1}), q is the electron's charge (q=1,602.10-19C) and T is the absolute temperature.

V_{OS} present the input offset voltage of the opamp.

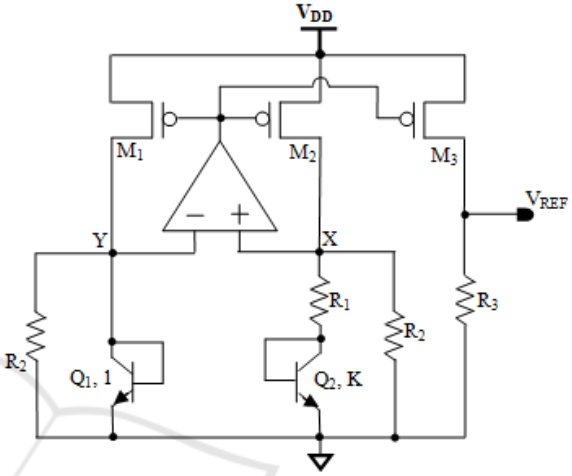

Figure 1: Schematic of Conventional sub-1V BGVR.

V_T has a positive temperature coefficient and represents the PTAT voltage. If we neglect the value of V_{OS}, the Equation 1 becomes:

$$V_{REF} = \frac{R_3}{R_2}.(V_{BE_1} + \frac{R_2}{R_1}.\ln K.V_T) \quad (3)$$

A voltage reference independent of the absolute temperature is obtained if $\frac{\partial V_{REF}}{\partial T} = 0$, then:

$$\frac{R_2}{R_1}.\ln K = -\frac{\partial V_{BE_1}/\partial T}{\partial V_T/\partial T} \quad (4)$$

Noted that $\frac{\partial V_{BE_1}}{\partial T} < 0$ and its value depends on the CMOS technology used and can be extracted by simulation, while $\frac{\partial V_T}{\partial T} > 0$ and it value can easily calculated.

The value of K is usually set to 8, so the resistor ratio $\frac{R_2}{R_1}$ can be calculated from Equation 4.

For a fixed value of V_{REF} less than 1V, the value of the resistance R_3 can be obtained from the Equation 3. Noted that the V_{REF} can be scaled by the resistor ratio $\frac{R_3}{R_2}$, and thus achieve an arbitrary V_{REF}.

The conventional sub-1V BGVR using opamp β-multiplier architecture ensures a low temperature coefficient for V_{REF} but remains very limited in terms of PSRR caused by the input offset voltage problem of the error amplifier, although some modifications have been proposed to improve the PSRR.

3 RELATED WORK

In order to achieve a high PSRR of the bandgap voltage reference, a pre-regulator scheme and low pass filter are added to a main circuit as shown in Figure 2 (Li and Zhang, 2014). The pre-regulator bloc improves a DC PSRR at low frequencies while the low pass filter improves a little the value of PSRR at high frequencies.

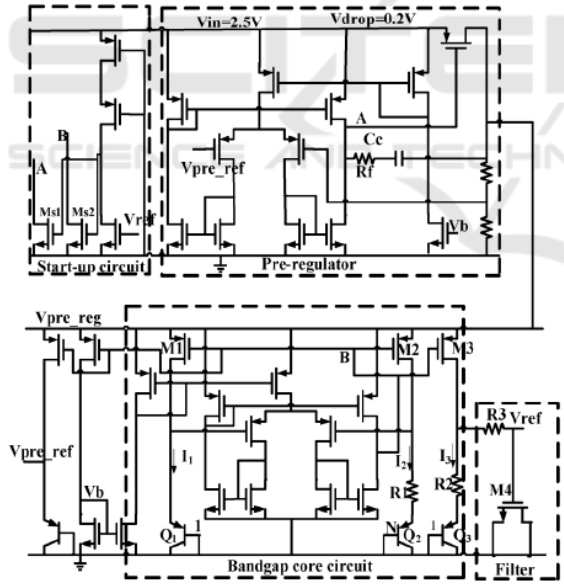

Figure 2: High PSRR structure of bandgap voltage reference proposed in (Li and Zhang, 2014).

The disadvantage of this structure is the use of large resistor to achieve a high PSRR and a low temperature coefficient.

4 PROPOSED SUB-1V BANDGAP VOLTAGE REFERENCE

The schematic of proposed sub-1V BGVR is shown in Figure 3. A current mode regulator scheme is inserted to improve the performance of the PSRR by isolating a supply voltage of the error amplifier and supply voltage of the BGVR core from a power supply source VDD.

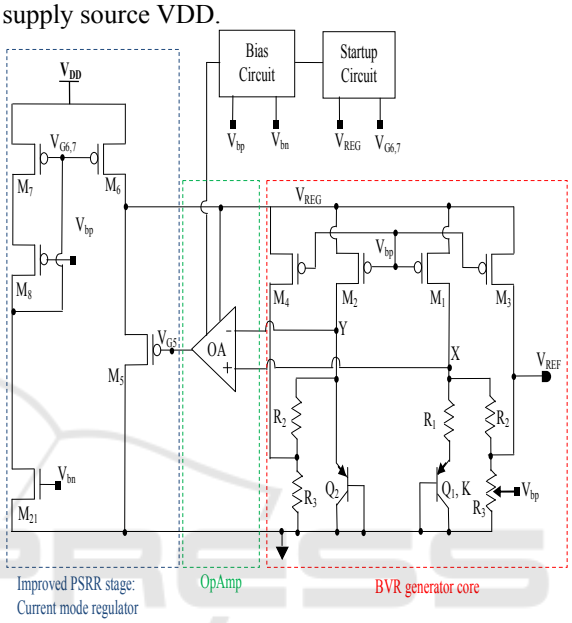

Figure 3: Schematic of proposed sub-1V BGVR

The schematic of the error amplifier used is shown in Figure 4, a self biased cascode current mirror load is adopted to achieve a high gain (Allen and Holberg, 2002). This opamp need a network compensation to achieve a sufficient phase margin to guarantee closed-loop stability.

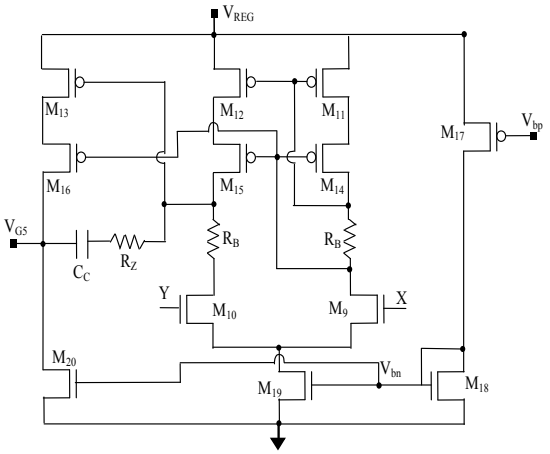

Figure 4: Schematic of error amplifier and his Bias circuit

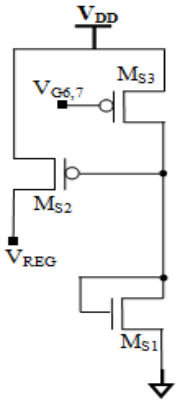

Figure 5: Schematic of Start-up circuit

The supply voltage of the opamp is V_{REG} which equal to regulate source-drain voltage of M_5. The proposed sub-1V BGVR needs a start-up circuit shown in Figure 5 to fix at the proper operation point.

4.1. Analysis and Design of Proposed BGVR Core

The core of the proposed BGVR uses the same principle of the conventional scheme with some modifications on the resistive voltage divider in order to compensate the error introduced by the input offset voltage of the error amplifier and consequently to have the same voltage level in the X and Y nodes.

The PMOS transistors M_1, M_2, M_3 and M_4 have identical size, such that the currents flowing through this four transistors are the same as $I_{D_1} = I_{D_2} = I_{D_3} = I_D$. The β-multiplier consists of two diode connected PNP transistors Q_1 and Q_2, with their emitter area ratio being K:1 to provide the required temperature dependent voltages to construct the voltage reference circuit.

The expression of the output voltage reference V_{REF} is given by:

$$V_{REF} = K_R .(V_{EB_2} + \frac{R_2}{2R_1}.U_T .\ln K + \frac{R_2}{2R_1}.V_{OS}) \quad (5)$$

With,

$$K_R = \frac{2R_3}{R_2 + 2R_3} \quad (6)$$

$$V_{REF} = K_R .(V_{EB_2} + \frac{R_2}{2R_1}.U_T .\ln K) \quad (7)$$

If we take into account the input offset voltage V_{OS}, we have $V_X = V_Y + V_{OS}$,

Thus the expression of V_{REF} becomes:

$$V_{REF} = K_R .(V_{EB_2} + \frac{R_2}{2R_1}.U_T .\ln K + \frac{R_2}{2R_1}.V_{OS}) \quad (8)$$

Equation 9 shows that the factor amplifying the input offset voltage is reduced in half in proposed circuit compared to that of the conventional scheme (see equation 1).

Differentiating equation 8 with respect to absolute temperature yields:

$$\frac{\partial V_{REF}}{\partial T} = K_R .(\frac{\partial V_{EB_2}}{\partial T} + \frac{R_2}{2R_1}.\ln K.\frac{\partial V_T}{\partial T}) \quad (9)$$

To achieve a near-zero TC of V_{REF}, $\frac{\partial V_{REF}}{\partial T} = 0$. Thus,

$$\frac{R_2}{2R_1}.\ln K = -\frac{\partial V_{EB_1}/\partial T}{\partial V_T/\partial T} \quad (10)$$

For the CMOS technology used in our design, $\frac{\partial V_{EB_2}}{\partial T} \approx 1.89\ mV/°C$, and by using Equation 2, we have $\frac{\partial V_T}{\partial T} = \frac{k_B}{q} \approx 0.0862\ mV/°C$, from where we get:

$$\frac{R_2}{2R_1}.\ln K = 21.9 \quad (11)$$

The value of K is close to 8, thus:

$$R_2 = 21.R_1 \quad (12)$$

The value of R_1 is calculated from the following equation:

$$R_1 = \frac{U_T .\ln K}{I_{PTAT}} \quad (13)$$

A reasonable current I_{PTAT} is designed to bias transistor Q_1 in the active region. The value of R_3 is

calculated from Equation 7 for a desired output voltage reference V_{REF}.

Design resistor example:

I_{PTAT}=10µA, $V_{EB_2} = 0.6\,V$, V_{REF}=0.65V.

We have: $$R_1 = \frac{U_T.\ln K}{I_{PTAT}}$$

We get: R_1=5.4 kΩ

From equation 12, we obtain: R_2=113.4 kΩ.

From equation 6 and 7, we have:

$$K_R = \frac{V_{REF}}{(V_{EB_2} + 21.U_T)}$$

We get: $K_R \approx 0.56$

Frome equation 6, we obtain: $R_3 = 0.64.R_2$

Thus: R_3=72.6 kΩ

Note that the final values of the resistances calculated by the hand must be adjusted during the design of the circuit to obtain an optimal value of the temperature coefficient of V_{REF} over the required temperature range.

The minimum supply voltage to ensure proper operation of the proposed circuit and obtain an output voltage reference V_{REF} less than 1 V with a small variation in the required temperature range is such that the following two constraints are met:

$$V_{DD} \geq V_{REF} + V_{SD_{sat\,3,4}} + V_{SD_{sat\,6,7}} \quad (14)$$

And,

$$V_{DD} \geq V_{EB_2} + V_{SD_{sat\,1,2}} + V_{SD_{sat\,6,7}} \quad (15)$$

Where $V_{SD_{sat\,3,4}}$ is the overdrive voltage of M_3 and M_4, $V_{SD_{sat\,1,2}}$ is the overdrive voltage of M_1 and M_2 and $V_{SD_{sat\,6,7}}$ is the overdrive voltage of M_6 and M_7.

4.2. PSRR Analysis

In order to reduce noise from the supply voltage which directly influences the performance of the PSRR, a pre-regulation stage is added to isolate the supply voltage V_{DD} from the supply voltage of the operational amplifier and also the supply voltage of the BGVR core generator.

To establish the expression of the PSRR, the high frequency small signal model of the proposed circuit is realised (see Figure 6). For the calculation of the PSRR, a similar method to that adopted in (Giustolisi and Palumbo, 2003) is applied. The body effect is ignored and both Q_1 and Q_2 BJT transistors can be considered as short-circuited.

The voltage v_{dif} shown in Figure 5 is the small signal part of the differential input voltage of the opamp.

We have:

$$PSRR(s) = \frac{v_{dd}(s)}{v_{ref}(s)} \quad (16)$$

Where $v_{dd}(s)$ is the high frequency small signal part of V_{DD}, $v_{ref}(s)$ is the high frequency small signal part of V_{REF} and s is the complex variable of Laplace.

We can write that:

$$PSRR(s) = \frac{v_{dd}(s)}{v_{reg}(s)} \times \frac{v_{reg}(s)}{v_{ref}(s)} \quad (17)$$

Where $v_{reg}(s)$ is the high frequency small signal part of V_{REG}.

For a simple notation the variable s is omitted in the voltages symbols.

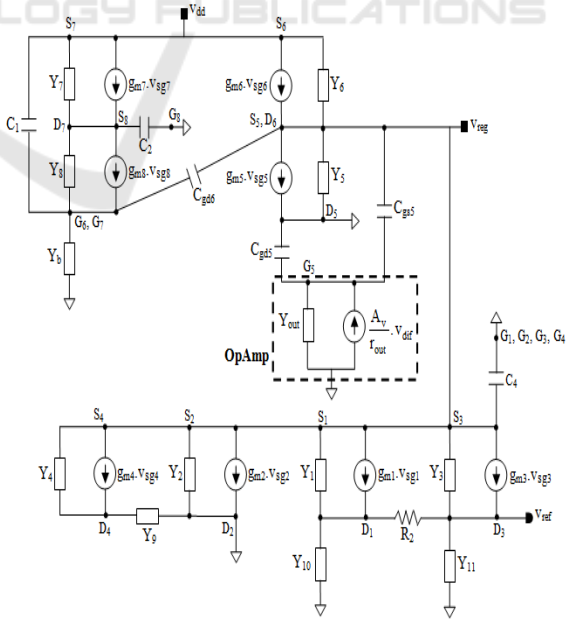

Figure 6: High frequency small signal model of proposed sub-1V BGVR

In the node D_3, the Kirchhoff's Current Law gives:

$$(g_{m_3}+Y_3).v_{reg}+R_2^{-1}.v_{d1}=(Y_3+Y_{11}+R_2^{-1}).v_{ref} \quad (18)$$

Where,

$$Y_3 = g_{03}+C_{ds3}.s \quad (19)$$

$$Y_{11} = R_3^{-1}+C_{gd3}.s \quad (20)$$

v_{d1} is the high frequency small signal part of V_{D1}.

In the node D_1, Kirchhoff's Current Law gives:

$$v_{d1} = \frac{(g_{m_1}+Y_1)}{(Y_1+Y_{10}+R_2^{-1})}.v_{reg}+\frac{R_2^{-1}}{(Y_1+Y_{10}+R_2^{-1})}.v_{ref} \quad (21)$$

Where,

$$Y_1 = g_{01}+C_{ds1}.s \quad (22)$$

$$Y_{10} = R_1^{-1}+C_{gd1}.s \quad (23)$$

By substituting equation 21 in equation 18, we obtain:

$$\frac{v_{reg}}{v_{ref}} = \frac{N_1(s)}{D_1(s)} \quad (24)$$

Where,

$$N_1(s) = (g_{m3}+Y_3).(Y_1+Y_{10}+R_2^{-1})+R_2^{-1}.(g_{m1}+Y_1) \quad (25)$$

$$D_1(s) = (Y_3+Y_{11}).(Y_1+Y_{10}+R_2^{-1})+R_2^{-1}.(Y_1+Y_{11}) \quad (26)$$

In the node D_6, the Kirchhoff's Current Law gives:

$$N_4(s).v_{reg} = Y_4.v_{d4}+Y_1.v_{d1}+Y_3.v_{ref}+(g_{m5}+Y_6).v_{dd}+(g_{m6}+C_{gd6}.s).v_{g6}+(g_{m5}+C_{gs5}.s).v_{g5} \quad (27)$$

Where,

$$N_4(s)=[g_{mT}+Y_T+g_{m5}+Y_5+Y_6+(C_{gd6}+C_{gs5}+C_4).s] \quad (28)$$

$$g_{mT} = g_{m1}+g_{m2}+g_{m3}+g_{m4} \quad (29)$$

$$Y_T = Y_1+Y_2+Y_3+Y_4 \quad (30)$$

$$Y_2 = g_{02}+C_{ds2}.s \quad (31)$$

$$Y_4 = g_{04}+C_{ds4}.s \quad (32)$$

$$Y_5 = g_{05}+C_{ds5}.s \quad (33)$$

$$Y_6 = g_{04}+C_{ds6}.s \quad (34)$$

$$C_4 = C_{gsl}+C_{gs2}+C_{gs3}+C_{gs4}+C_{bsl}+C_{bs2}+C_{bs3}+C_{bs4} \quad (35)$$

And, v_{d4} is the high frequency small signal part of V_{D4}, v_{g5} is the high frequency small signal part of V_{G5} and v_{g6} is the high frequency small signal part of V_{G6}.

In the node D_4, the Kirchhoff's Current Law gives:

$$v_{d4} = \frac{(g_{m_4}+Y_4)}{(Y_1+Y_9)}.v_{reg} \quad (36)$$

Where,

$$Y_9 = (R_2//R_3)^{-1}+C_{gd4}.s \quad (37)$$

In the node G_5, Kirchhoff's Current Law gives:

$$v_{g5} = \frac{A_v}{r_{out}.[Y_{out}+(C_{gd5}+C_{gs5}).s]}.v_{d1}+\frac{C_{gs5}.s}{[Y_{out}+(C_{gd5}+C_{gs5}).s]}.v_{reg} \quad (38)$$

Where,

$$Y_{out} = r_{out}^{-1}+C_{out}.s \quad (39)$$

A_v is the open-loop gain of the opamp and r_{out} is its output resistance.

C_{out} is all capacitance connected from the output of the opamp to ground.

In the node G_6, the Kirchhoff's Current Law gives:

$$[Y_b+(C_1+C_{gd6}).s].v_{g6} = C_1.s.v_{dd}+C_{gd6}.v_{reg}+(g_{m8}+Y_8).v_{s8} \quad (40)$$

Where, v_{s8} is the high frequency small signal part of V_{S8} and,

$$Y_b = R_b^{-1}+C_{gd8}.s \quad (41)$$

Where R_b represent the output resistance of current source bias network and,

$$C_1 = C_{gs6} + C_{gs7} + C_{bs6} + C_{bs7} \quad (42)$$

$$Y_8 = g_{08} + C_3 . s \quad (43)$$

$$C_3 = C_{ds8} + C_{gd7} \quad (44)$$

In the node S_8, the Kirchhoff's Current Law gives:

$$v_{s8} = \frac{(g_{m7} + Y_7)}{(g_{m8} + Y_8 + Y_7 + C_2 . s)} . v_{dd} + \frac{(Y_8 - g_{m7})}{(g_{m8} + Y_8 + Y_7 + C_2 . s)} . v_{g6} \quad (45)$$

Where,

$$C_2 = C_{gs8} + C_{ds8} \quad (46)$$

By substituting equation 45 in equation 40, we obtain:

$$v_{g6} = \frac{N_2(s)}{D_2(s)} . v_{dd} + \frac{N_3(s)}{D_2(s)} . v_{reg} \quad (47)$$

Where,

$$N_2(s) = C_1 . s(g_{m8} + Y_7 + Y_8 + C_2 . s) + (g_{m8} + Y_8).(g_{m7} + Y_7) \quad (48)$$

$$N_3(s) = C_{gd6} . s(g_{m8} + Y_7 + Y_8 + C_2 . s) \quad (49)$$

$$D_2(s) = [Y_b + (C_1 + C_{gd6}).s)].(g_{m8} + Y_8 + Y_7 + C_2 . s) + (g_{m7} - Y_8).(g_{m8} + Y_7) \quad (50)$$

By substituting equations 21, 36, 38 and 47 in equation 27, we obtain:

$$\frac{v_{reg}}{v_{dd}} = \frac{(g_{m5} + g_{m6} + Y_6 + C_{gd6} . s).N_2(s).D_3(s).D_1(s)}{D_4(s) - [D_5(s) + D_6(s) + D_7(s) + D_8(s)]} \quad (51)$$

Where,

$$D_4(s) = N_4(s).D_3(s).D_1(s).D_2(s) \quad (52)$$

$$D_5(s) = D_1(s).D_3(s). \left[\frac{D_2(s).Y_4.(g_{m4} + Y_4)}{(Y_4 + Y_9)} + N_3(s).(g_{m6} + C_{gd5} . s) \right] \quad (53)$$

$$D_6(s) = D_1(s).D_2(s).Y_1.(g_{m1} + Y_1).r_{out} . [Y_{out} + (C_{gd5} + C_4).s] \quad (54)$$

$$D_7(s) = D_1(s).D_2(s).(g_{m5} + C_4 . s). [A_v .(g_{m1} + Y_1) + r_{out}.(Y_1 + Y_{10} + R_2^{-1}).C_4 . s] \quad (55)$$

$$D_8(s) = N_1(s).D_2(s). \left\{ r_{out}.Y_1.R_2^{-1}.[Y_{out} + (C_{gd5} + C_4).s] + Y_3.D_3(s) + (g_{m5} + C_4 . s).A_v . R_2^{-1} \right\} \quad (56)$$

Note that g_{0i} represents the small signal source-drain conductance of the MOSFET M_i and Y_i represents the equivalent admittance for the shunt connection of the impedance of the capacitor and a resistor.

By substituting equations 24 and 51 in equation 17, we obtain:

$$PSRR(s) = \frac{(g_{m5} + g_{m6} + Y_6 + C_{gd6} . s).N_2(s).D_3(s).N_1(s)}{D_4(s) - [D_5(s) + D_6(s) + D_7(s) + D_8(s)]} \quad (57)$$

The expression of the PSRR(s) shows that its transfer function has 7 poles and 7 zeros, and consequently the frequency response is convergent and the proposed circuit system is stable.

The expression of DC value (zero frequency) of the PSRR is obtained by replacing s=0 in all the terms containing the complex variable s. Thus,

$$PSRR(0) = \frac{(g_{m5} + g_{m6} + g_{06}).N_2(0).D_3(0).N_1(0)}{D_4(0) - [D_5(0) + D_6(0) + D_7(0) + D_8(0)]} \quad (58)$$

The equation 58 shows that the DC value of PSSR can be improved by more than 20dB in comparison to the previous high PSRR structures in related work (Li and Zhang, 2014; Tham and Nagaraj, 1995; Francisco and Hora, 2012).

5 SIMULATION RESULTS AND LAYOUT

The proposed design of sub-1V bandgap voltage reference was simulated in 0.18-µm CMOS 1.8V/3.3V technology using Cadence Virtuoso Spectre Simulator. The proposed circuit generates an output voltage reference V_{REF} of 0.6346 V at 27°C when the supply voltage is set to 1.8V. As it is shown in Figure 7, the measurement temperature coefficient of V_{REF} is 22,3ppm/°C over temperature range -40°C to 140°C.

Table 1: Simulation results summary and comparison

Performance	[17]	[18]	[19]	This work
Technology (CMOS)	0,9 µm	0.09 µm	0.18 µm	0.18 µm
$V_{DD,min}$ (V)	2.7	2.6	2.5	1.2
$V_{DD,max}$ (V)	5.5	3.6	6	1.8
V_{REF} (V)	1.236	0.21398	1.194	0.6346
TC (ppm/°C)	85	6.07	6.51	22.3
Temperature operation range (°C)	-50 to 125	-20 to 120	-25 to 80	-40 to 140
Line regulation		20µV/V	1143µV/V	104µV/V
PSRR DC (dB)	-80	-82.7	-125	-93
PSRR@ 1MHz	-40		-40	-71
PSRR@ 10MHz				-52.8

As it is shown in Figure 8 the DC value of PSRR is -93dB at 10 kHz and -71dB at 1MHz is achieved. The measurement line regulation of V_{REF} is 104µV/V as it is shown in Figure 9.

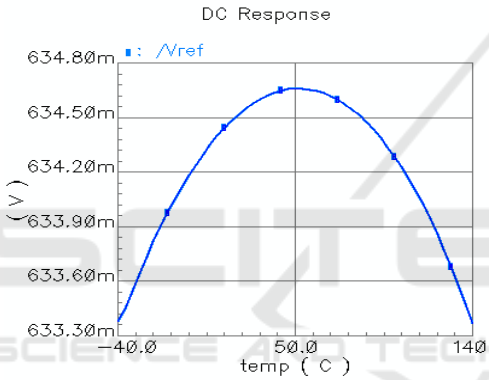

Figure 7: Simulated temperature dependence of the output voltage reference at 1.8 supply voltage.

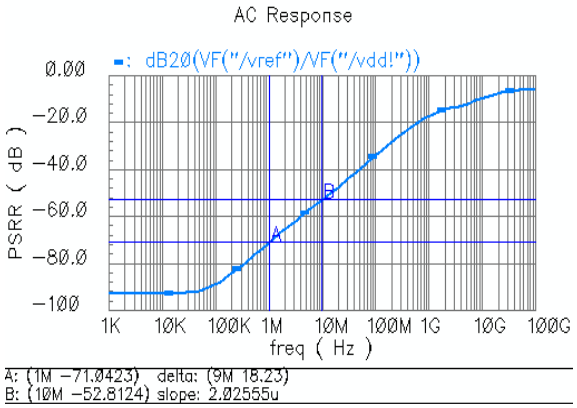

Figure 8: Simulated PSRR of the proposed sub-1V BGVR.

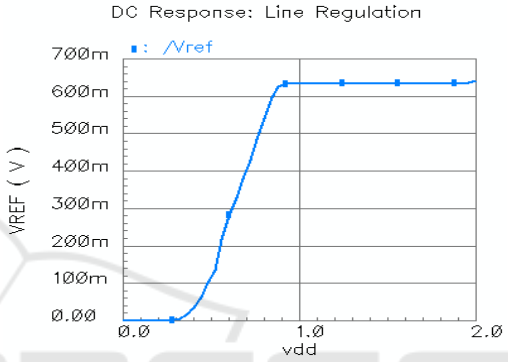

Figure 9: Simulated line regulation of the proposed sub-1V BGVR.

Table 1 summarizes performance characteristics of the proposed sub-1V BGVR and comparison with related works is given. As shown in Table I, the proposed circuit satisfied the high performance of a voltage reference and especially for the PSRR value in the 1MHz to 10MHz frequency range which is significantly higher than the value found in the related works (see Table 1).

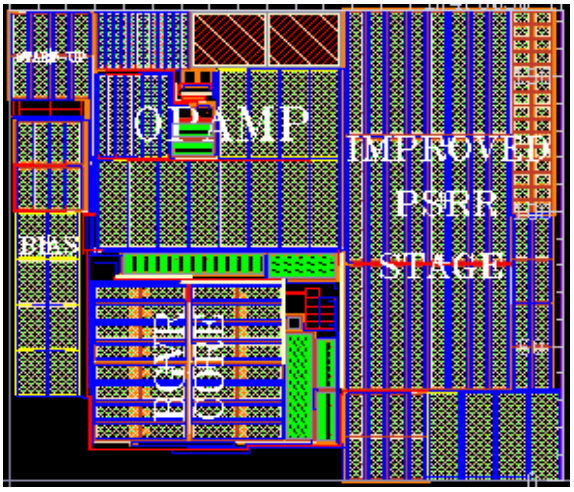

Figure 10: Layout of proposed sub-1V BGVR reference

The layout of the proposed sub-1V bandgap voltage reference is shown in Figure 10, the area is 0.0337 mm^2.

6 CONCLUSIONS

In this paper a novel design of sub-1V bandgap voltage reference circuit with opamp base β-multiplier and resistive divider architecture is proposed. The important contribution of this work is the obtaining of an accurate voltage reference value with a high value of the PSRR in a very wide frequency range from 1kHz up to 10MHz.

The proposed architecture of the voltage divider has made it possible to minimize the undesirable effect of the input offset voltage of the opamp and consequently to obtain a very accurate value of the output voltage and to improve the dc value of the PSRR.

In order to reduce noise from the supply voltage which directly influences the performance of the PSRR, a pre-regulation stage is added to isolate the supply voltage source from the supply voltage of the operational amplifier and also the supply voltage of the BGVR core generator which allows improving the value of the PSRR in high frequency.

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