ECG Pattern Recognition and Beat Classification using Internet of Things and Hardware Acceleration on ZynQ (SOC) Platform with High Performance Computational PCIe Protocol

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Keywords: ZynQ System on Chip (SoC), Internet of Things (IoT), Think Speak Cloud, Object Identification, Dynamic Reconfigure Port (DRP), Transmission Control Protocol/Internet Protocol, Peripheral Component Interconnect Express (PCIe), Direct Memory Access.

Abstract: The ECG signals plays an important vital role in Diagnostics Systems. The Real time Hardware Implementation Provides Accuracy, speed, Beat classification, predictivity and diagnostics of the system Interpretation and classification The ECG Signal extraction from sensor and Processing on the Zynq SoC Platform and Imported on to the cloud in involves three Steps: i) Real time data fetch from the Sensor device ii) Pushing on to the Cloud uproot Using TCP/IP Protocol iii) Cloud IDE Processing Using SDAccel openCL language with Amazon FPGA Image (AFI) on Virtual servers with the help of openCL/C++ libraries, Xilinx SDx Environments and virtual JTAG interfaces on Xilinx Virtex Ultrascale Plus Board(VU9P) low profile PCIe accelerated Board.

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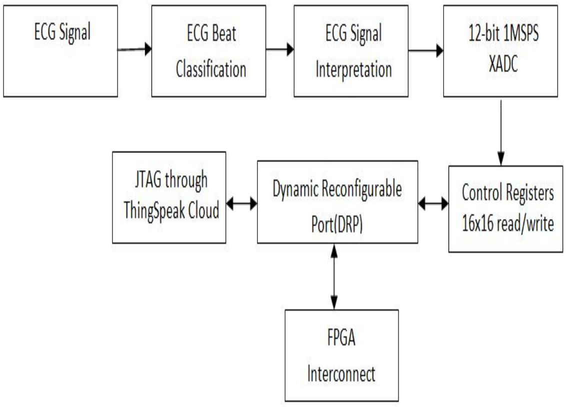
1 INTRODUCTION

ECG signal are important for detection of crucial heart diseases and Continues monitoring system will help in identification of prolonged chest pain and other related diseases like heart attack stages and their Symptoms. There are different diagnostics systems like holter monitor, traditional diagnostics systems.

ECG beat annotation signals provides the information on chemical imbalance, prolonged medication and drug addictions. There are different algorithm like Partial swam Optimization (PSO), Fuzzy models, ANFIS provides that better analysis and realistic outputs.

2 METHODOLOGY

1. IoT Based ECG Analog input signal from XADC port or using sensors Temperature transmission using ZynQ Board
2. Loading the ECG Signals from SDcard (Standalone) from ThingSpeak Cloud
3. Transmitting Through the UDP Port
4. Processing the ECG Signals from Python Yolo frame work and Filtering the ECG Signals.
5. DMA using PCIe Implementation Using Xilinx Vivado IP based design and SDK Environment.
6. Cloud IDE Processing Using SDAccel openCL language with Amazon FPGA Image (AFI).
7. Virtual servers with the help of openCL/C++ libraries, Xilinx SDx Environments and virtual JTAG interfaces on Xilinx Virtex Ultrascale Plus Board(VU9P) low profile PCIe accelerated Board.


ECG Signal
ECG Beat Classification
ECG Signal Interpretation
12-bit 1MSPS XADC
JTAG through ThingSpeak Cloud
Dynamic Reconfigurable Port(DRP)
Control Registers 16x16 read/write
FPGA Interconnect

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2.1 Operations

i) XADC performs Analog to Digital Conversion, ii) Measure the Onchip Temperatures and Voltages , iii) Set alarms for performance.

2.2 Interface Supports

- AXI4 lite
- Dynamic Reconfigurable Port (DRP)
- AXI Stream

Loading the ECG signals in Analog Sim options in DRP Timing panel, You can able to load the CSV or text file consists of Integer values.

The Re-customization of XADC Wizard Consists of two ADC Converts in that one for Temperature sensor and another for External Analog ECG signals and Multiplexed with 12-bit 1MSPS resolution of data conversion and loading on to the Registers banks

The Sensors will detect the On chip temperatures, Voltages of the Chip, Dual 12 bit 1MSPS XADC port (Analog to Digital Converter) as Vp_0, Vn_0, Vauxp[0], Vauxn[0] and Voltage Sensor pins. XADC in Zynq 7000 series will have different sensors to Check Voltages and Temperature of the chip die. Zynq SoC will have different banks, in that XADC pins are located in Bank 0. Dynamic Reconfigure Port via interface to JTAG to download the bit file. The Block of XADC port as shown below in figure 1.

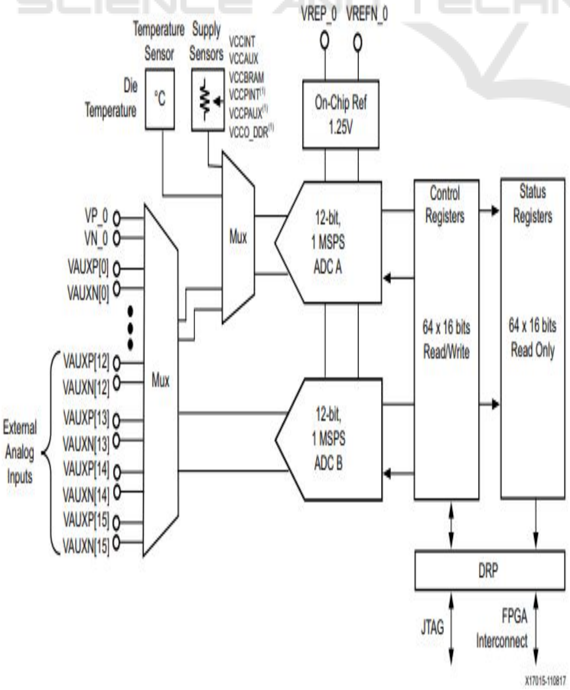

Figure 1: Block diagram of XADC wizard.

The Entire Implementation of ECG Beat Annotation signals and their Classification Using Yolo framework using Bayesian classifier.

The ECG signals conversion using Xilinx Vivado tool with Zynq SOC Platform for Implementation. I) Zynq Processor acts like master and rest acts like Peripherals AXI4 Lite, XADC wizard, On top of it Application code to check the ECG Beat annotation signals.

Xilinx Vivado software is used for Implementation with IP block design, Conversion of IP design into RTL code using HDL wrappers, shown below figure 2.

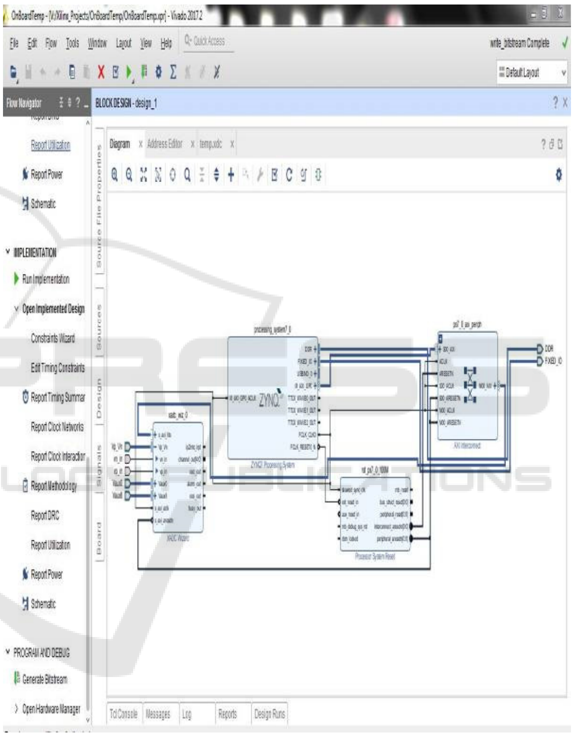

Figure 2: Block design Implementation.

Zynq SOC 7000 series ZedBoard act like a prototyping devices. Where Synthesis, Implement the design and Generate the bit file to download on to the Board.

The IP Based design acts like a building block on the top OS we need to write an application code C-code to build the SOC system,

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The Program Code as follows-

```
Application Code:
#include <stdio.h>
#include "platform.h"
#include "xsysmon.h"
#defineSYSMON_DEVICE_ID
XPAR_SYSMON_0_DEVICE_ID
#define XSysMon_RawToExtVoltage(AdcData) \
((((float)(AdcData))*(1.0f))/65536.0f)  //(ADC  16bit
result)/16/4096 = (ADC 16bit result)/65536
 // voltage value = (ADC 16bit result)/65536 * 1Volt
static XSysMon SysMonInst; //a sysmon instance
static int SysMonFractionToInt(float FloatNum);
int main()
{
 u8 SeqMode;
 u32
TempRawData,VccIntRawData,ExtVolRawData,i;
 float TempData,VccIntData,ExtVolData;
 int xStatus;
 XSysMon_Config *SysMonConfigPtr;
 XSysMon *SysMonInstPtr = &SysMonInst;
init_platform();
 print("Hello World\n\r");
 SysMonConfigPtr                                  =
XSysMon_LookupConfig(SYSMON_DEVICE_ID)
;
 if(SysMonConfigPtr            ==             NULL)
printf("LookupConfig FAILURE\n\r");
 xStatus  =  XSysMon_CfgInitialize(SysMonInstPtr,
SysMonConfigPtr,SysMonConfigPtr->BaseAddress)
;
 if(XST_SUCCESS != xStatus) printf("CfgInitialize
FAILED\r\n");
XSysMon_GetStatus(SysMonInstPtr);  //  Clear  the
old status
 while(1)
 { //wait until EOS activated
while    ((XSysMon_GetStatus(SysMonInstPtr)    &
XSM_SR_EOS_MASK)                               !=
XSM_SR_EOS_MASK);

TempRawData                                       =
XSysMon_GetAdcData(SysMonInstPtr,
XSM_CH_TEMP);//Read  the  on-chip  Temperature
Data
 TempData                                         =
XSysMon_RawToTemperature(TempRawData);
 printf("\r\nThe  Current  Temperature  is  %0d.%03d
Centigrades.\r\n",
 (int)(TempData),
SysMonFractionToInt(TempData));
```

Synthesis output as shown in the figure 3.

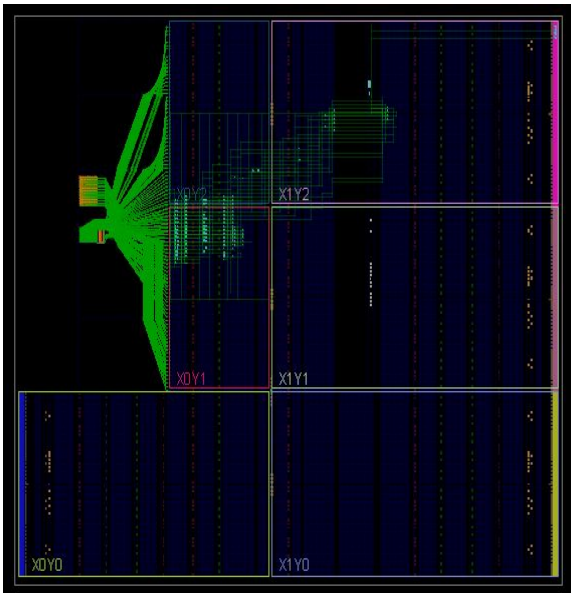
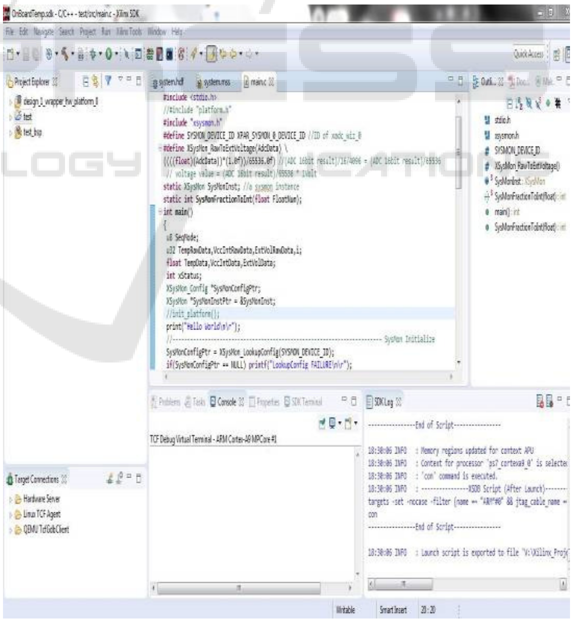


Figure 3: Hardware Implementation in PS section.

The Implementation stage the Utilization of area and Power Consumption reports. XADC banking regions shown in figure 3.


OnBoardTemp.sdk - C/C++ - test/src/main.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Tools Window Help
Quick Access
Project Explorer
design_1_wrapper_hw_platform_0
test
test_bsp
system.hdf
system.mss
main.c
Outl...
stdio.h
xsysmon.h
SYSMON_DEVICE_ID
XSysMon_RawToExtVoltage()
SysMonInst : XSysMon
SysMonFractionToInt(float) : int
main() : int
SysMonFractionToInt(float) : int
Problems
Tasks
Console
Properties
SDK Terminal
TCF Debug Virtual Terminal - ARM Cortex-A9 MPCore #1
SDK Log
Target Connections
Hardware Server
Linux TCF Agent
QEMU TcfGdbClient
Writable
Smart Insert
20 : 20

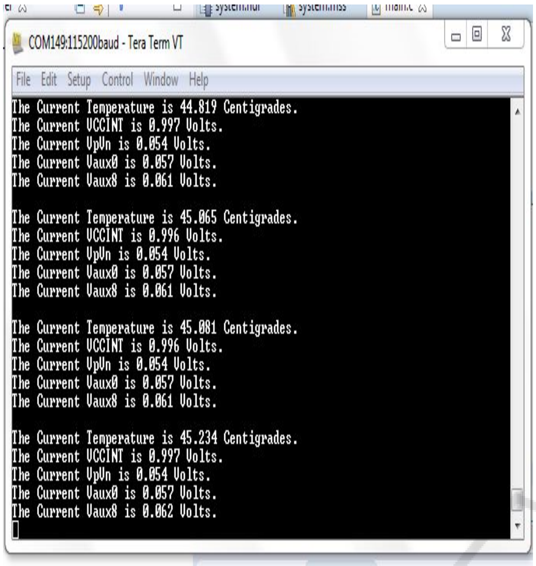
```
#include <stdio.h>
//#include "platform.h"
#include "xsysmon.h"
#define SYSMON_DEVICE_ID XPAR_SYSMON_0_DEVICE_ID //ID of xadc_wiz_0
#define XSysMon_RawToExtVoltage(AdcData) \
((((float)(AdcData))*(1.0f))/65536.0f) //(ADC 16bit result)/16/4096 = (ADC 16bit result)/65536
 // voltage value = (ADC 16bit result)/65536 * 1Volt
static XSysMon SysMonInst; //a sysmon instance
static int SysMonFractionToInt(float FloatNum);
int main()
{
 u8 SeqMode;
 u32 TempRawData,VccIntRawData,ExtVolRawData,i;
 float TempData,VccIntData,ExtVolData;
 int xStatus;
 XSysMon_Config *SysMonConfigPtr;
 XSysMon *SysMonInstPtr = &SysMonInst;
 //init_platform();
 print("Hello World\n\r");
 //---------------------------------------------------------------- SysMon Initialize
 SysMonConfigPtr = XSysMon_LookupConfig(SYSMON_DEVICE_ID);
 if(SysMonConfigPtr == NULL) printf("LookupConfig FAILURE\n\r");
```

```
---------------End of Script---------------

18:38:06 INFO  : Memory regions updated for context APU
18:38:06 INFO  : Context for processor 'ps7_cortexa9_0' is selecte
18:38:06 INFO  : 'con' command is executed.
18:38:06 INFO  : ---------------XSDB Script (After Launch)-------
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =
con
---------------End of Script---------------

18:38:06 INFO  : Launch script is exported to file 'V:\Xilinx_Proj
```

Figure 4: Application code in SDK platform.

The C-Code Implemented on Xilinx SDK Platform as shown above and the Communication using JTAG Port.

The Serial Terminal using Board rate as 115200, we can able to communicate the design Analog ECG signals and Print on the XADC ICAP Port.

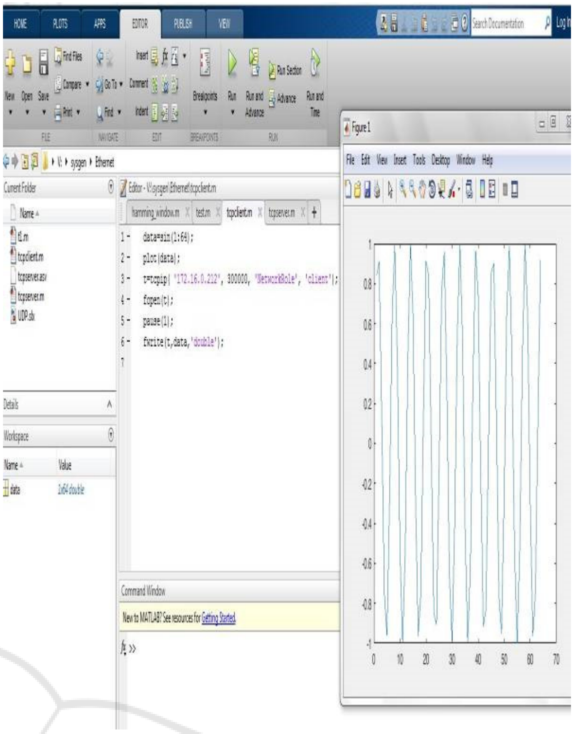

COM149:115200baud - Tera Term VT
File Edit Setup Control Window Help

```
The Current Temperature is 44.819 Centigrades.
The Current VCCINT is 0.997 Volts.
The Current VpVn is 0.054 Volts.
The Current Vaux0 is 0.057 Volts.
The Current Vaux8 is 0.061 Volts.

The Current Temperature is 45.065 Centigrades.
The Current VCCINT is 0.996 Volts.
The Current VpVn is 0.054 Volts.
The Current Vaux0 is 0.057 Volts.
The Current Vaux8 is 0.061 Volts.

The Current Temperature is 45.081 Centigrades.
The Current VCCINT is 0.996 Volts.
The Current VpVn is 0.054 Volts.
The Current Vaux0 is 0.057 Volts.
The Current Vaux8 is 0.061 Volts.

The Current Temperature is 45.234 Centigrades.
The Current VCCINT is 0.997 Volts.
The Current VpVn is 0.054 Volts.
The Current Vaux0 is 0.057 Volts.
The Current Vaux8 is 0.062 Volts.
```

Figure 5: UART real time processed data on FPGA.

The ECG Signal from ADC port pushing on to the serial port of Zynq SOC using Matlab Software and Convert it as Character.

UDP is a Communication Protocol between the networks, UDP works on four parameters like Source port, destination port, length and Check sum. Implementation of UDP Protocol in simulink design Using Real time Simulink explorer , UDP send block, Receive block in the design. UDP doesn't have an order to track the packets. so TCP/IP protocol is Implemented in Communication channel to overcome the packet loss. To Overcome the packet loss, we use TCP/IP protocol. Transmission Control Protocol is a communication channel between Application layer and transport layer. Basically it work s on the functionality of Byte Streaming, Connection Oriented, Full duplex, Piggy Backing, error control, flow control and conjuction control Mechanism. TCP/IP first priority is to segment the obtained data from application layer. It works over Three way hand shaking. Because of which guarantees the no loss data. Implemented using MATLAB Script file in two stages as : Transmission server and client based Remote desktop machines. Whenever the data is sent to the receiver the flow should be followed, otherwise receiver will overflow due to huge data and might be data loss.



```
data=sin(1:64);
plot(data);
t=tcpip('172.16.0.212', 300000, 'NetworkRole', 'client');
fopen(t);
pause(1);
fwrite(t,data,'double');
```

New to MATLAB? See resources for Getting Started.

Figure 6: TCP/IP client received signal.

Finally Upload the ECG Annotation signal on to the Think Speak Cloud to print the live Signals.

XADC wizard in Xilinx Artix7 FPGA has to convert ADC. It has Voltage and on chip Temperature Sensor which will monitor the FPGA device. We Created Zynq Ps and for PL we create XADC IP. We write an application for the hardware XADC for On chip temp sensor. We read the temperature value from UART by PS side. Through Matlab and ThingSpeak we can read the data from the Xilinx SDK Application and Update it in the ThingSpeak Cloud.

3 DMA FOR PCIE

Direct Memory access for Peripheral Component Interface Express (PCIe)

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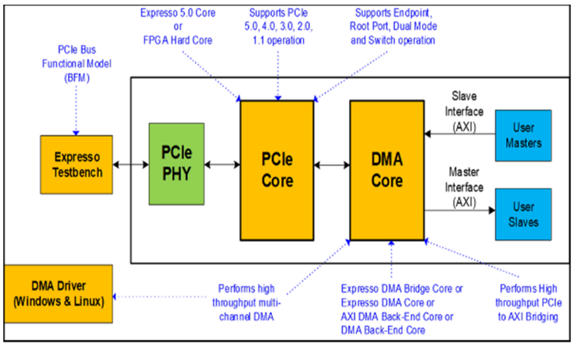
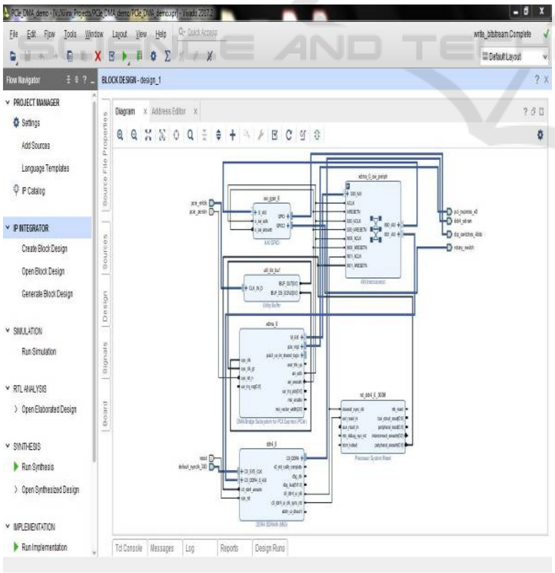

Expresso 5.0 Core or FPGA Hard Core
Supports PCIe 5.0, 4.0, 3.0, 2.0, 1.1 operation
Supports Endpoint, Root Port, Dual Mode and Switch operation
PCIe Bus Functional Model (BFM)
Expresso Testbench
PCIe PHY
PCIe Core
DMA Core
Slave Interface (AXI)
User Masters
Master Interface (AXI)
User Slaves
DMA Driver (Windows & Linux)
Performs high throughput multi-channel DMA
Expresso DMA Bridge Core or Expresso DMA Core or AXI DMA Back-End Core or DMA Back-End Core
Performs High throughput PCIe to AXI Bridging

Figure 7: Thing Speak Cloud with ECG Uploads as follows.

Advanced eXtensible Interconnect AXI4 -stream, will provides upto 4 read & 4 write channels. 64/128/256 bit data bus up to 250Mhz Scattered Block engine.

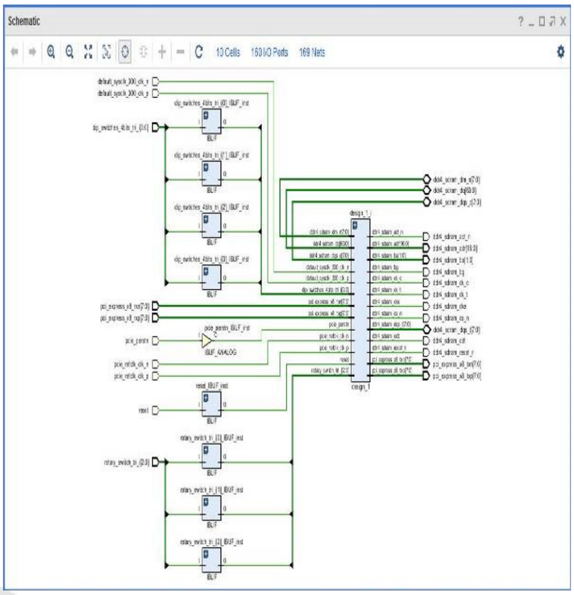
Implementation of DMA for PCIe using KCU105 board having PCIe slot connect to the host server systems.

It provides Communication between Host to PCIe Card & Card to Host machine. The Hardware Blocks involved are AXI GPIO, DMA/Bridge Subsystem for PCI Express, AXI Performance Monitor, AXI BRAM, System ILA, System Management Wizard, DDR4 SDRAM, Block Memory Generator, Processing System, and AXI Interconnect block in Vivado IPI based Model as shown below.



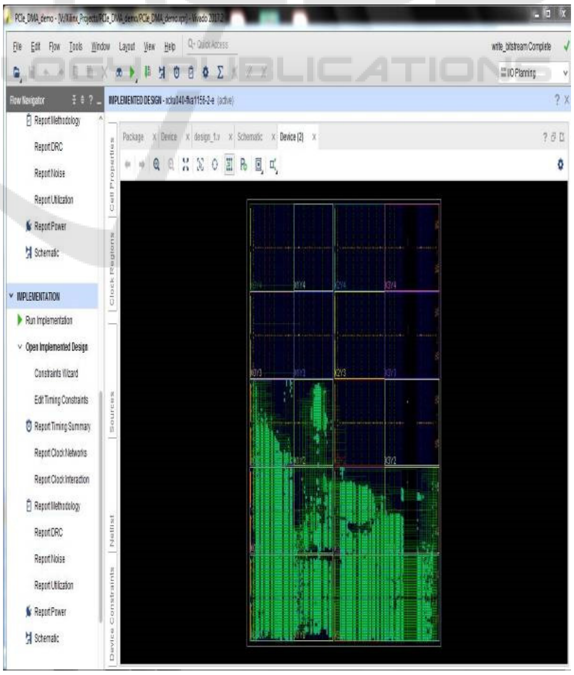
The IPI blocks are Validated with no errors, Generated input-output products to ger the RTL-Verilog code for synthesis and Implementation stage followed by bit file generation and HDF file.

The Schematic Design



Exporting it into Software Development platform (SDK) Application in C-code to control the API design.

Design Implementation Stage



Resource Utilization of Hardware system.

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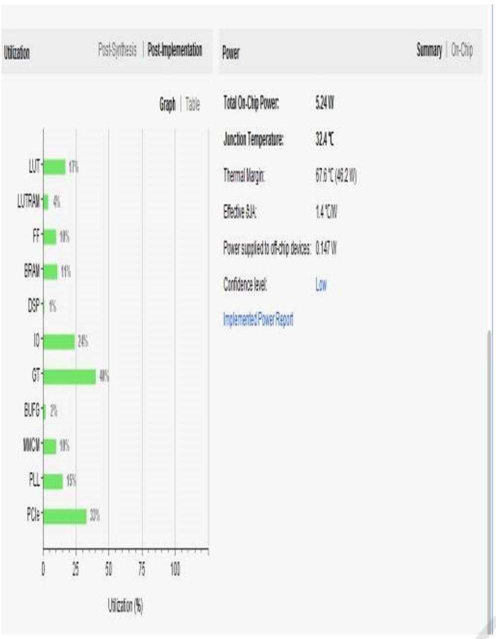
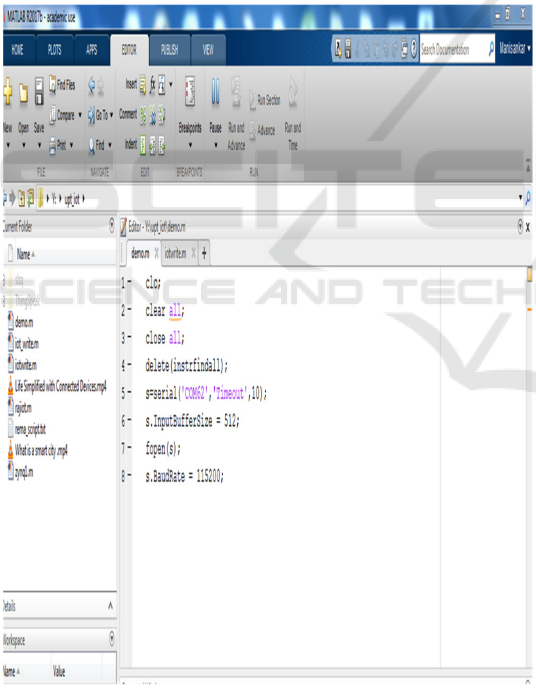
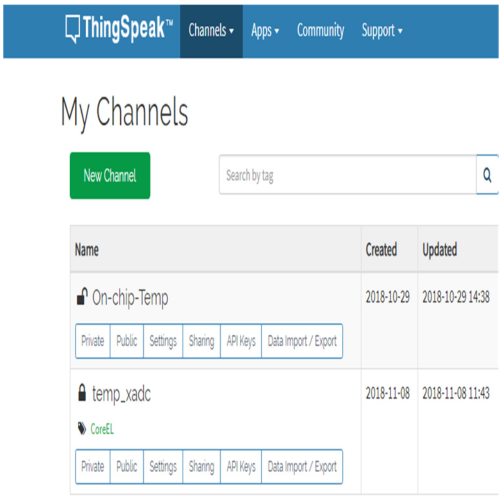


Power | Summary | On-Chip

Total On-Chip Power: 5.24 W
Junction Temperature: 32.4 °C
Thermal Margin: 67.6 °C (46.2 W)
Effective θJA: 1.4 °C/W
Power supplied to off-chip devices: 0.147 W
Confidence level: Low
Implemented Power Report



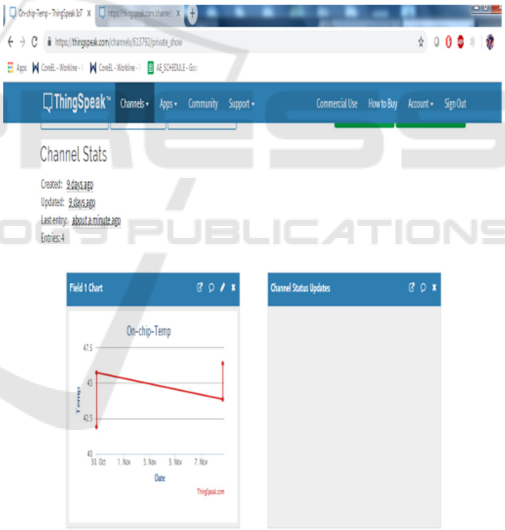
```
clc;
clear all;
close all;
delete(instrfindall);
s=serial('COM62','Timeout',10);
s.InputBufferSize = 512;
fopen(s);
s.BaudRate = 115200;
```



Name	Created	Updated
On-chip-Temp	2018-10-29	2018-10-29 14:38
temp_xadc	2018-11-08	2018-11-08 11:43

Figure 8: ThinkSpeak Cloud Channels.

The Uploaded ECG signals are Processed by Yolo Frame work Python design using Bayesian Classifier to identify the ECG Annotation Signals.



Channel Stats

Created: 9 days ago
Updated: 9 days ago
Last entry: about a minute ago
Entries: 4

Figure 9: Real time data transfer on MATLAB cloud.

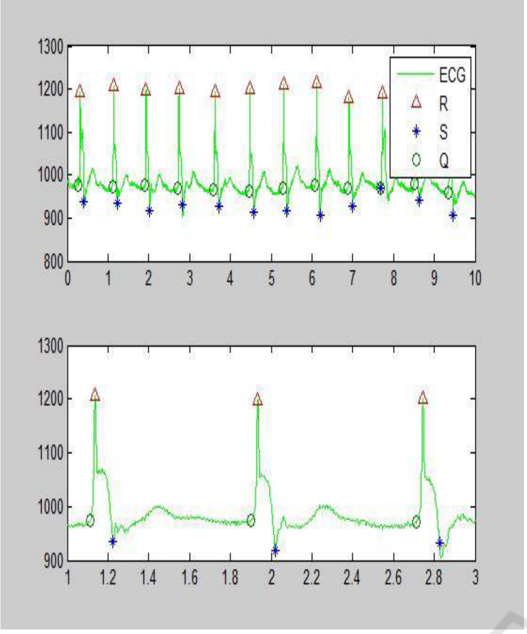
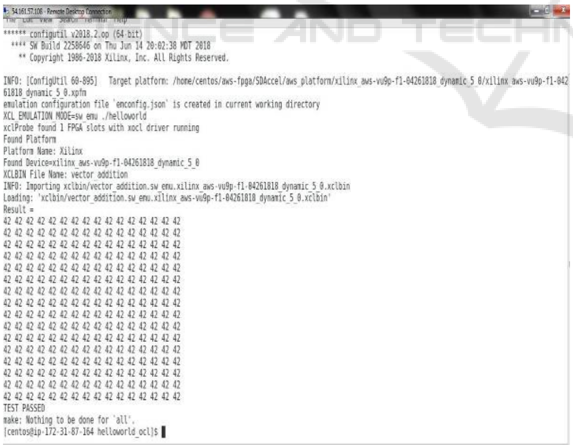


Figure 10: ECG Annotation signals on Cloud.

Cloud Computing Solutions with AWS

Virtual servers with the help of openCL/C++ libraries, Xilinx SDx Environments and virtual JTAG interfaces on Xilinx Virtex Ultrascale Plus Board(VU9P) low profile PCIe accelerated Board.



```
****** configutil v2018.2.op (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

INFO: [ConfigUtil 60-895]   Target platform: /home/centos/aws-fpga/SDAccel/aws_platform/xilinx_aws-vu9p-f1-04261818_dynamic_5_0/xilinx_aws-vu9p-f1-042
61818_dynamic_5_0.xpfm
emulation configuration file `emconfig.json` is created in current working directory
XCL_EMULATION_MODE=sw_emu ./helloworld
xclProbe found 1 FPGA slots with xocl driver running
Found Platform
Platform Name: Xilinx
Found Device=xilinx_aws-vu9p-f1-04261818_dynamic_5_0
XCLBIN File Name: vector_addition
INFO: Importing xclbin/vector_addition.sw_emu.xilinx_aws-vu9p-f1-04261818_dynamic_5_0.xclbin
Loading: 'xclbin/vector_addition.sw_emu.xilinx_aws-vu9p-f1-04261818_dynamic_5_0.xclbin'
Result =
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
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42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
42 42 42 42 42 42 42 42 42 42 42 42 42 42 42 42
TEST PASSED
make: Nothing to be done for `all'.
[centos@ip-172-31-87-164 helloworld_ocl]$ ▌
```
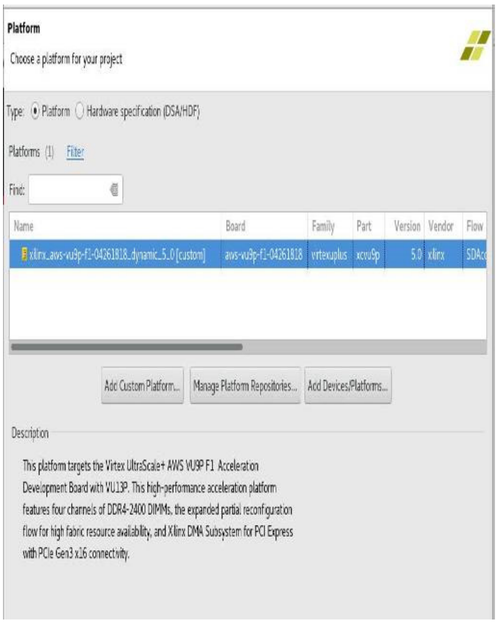

The platform targets the Virtex Ultrascale + AWS amazon Web services VU9P F1 acceleration Development with VU13P. The high Performance acceleration platform features four channels of DDR4-2400 DIMMs, the expanded partial reconfiguration flow for high fabric resource availability and Xilinx DMA subsystem for PCIe Express with PCIe Gen 3x16 connectivity.



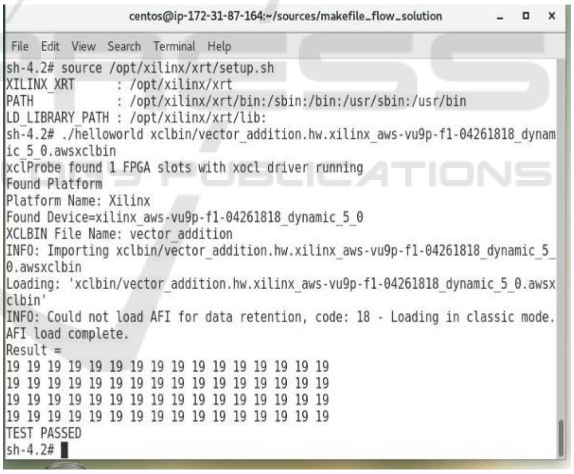
Type: ● Platform ○ Hardware specification (DSA/HDF)

Name	Board	Family	Part	Version	Vendor	Flow
xilinx_aws-vu9p-f1-04261818_dynamic_5_0 [custom]	aws-vu9p-f1-04261818	virtexuplus	xcvu9p	5.0	xilinx	SDAcc

This platform targets the Virtex UltraScale+ AWS VU9P F1 Acceleration Development Board with VU13P. This high-performance acceleration platform features four channels of DDR4-2400 DIMMs, the expanded partial reconfiguration flow for high fabric resource availability, and Xilinx DMA Subsystem for PCI Express with PCIe Gen3 x16 connectivity.

Figure 11: SDx Environment with Hardware XU9P.

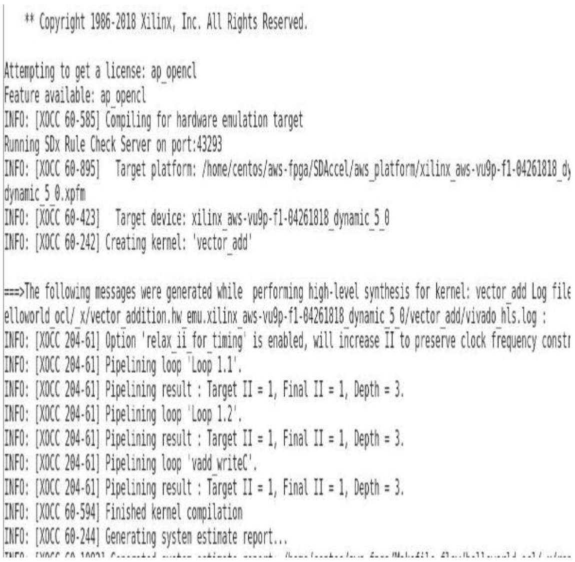
AFI Data Retension


centos@ip-172-31-87-164:~/sources/makefile_flow_solution
File Edit View Search Terminal Help

```
sh-4.2# source /opt/xilinx/xrt/setup.sh
XILINX_XRT      : /opt/xilinx/xrt
PATH            : /opt/xilinx/xrt/bin:/sbin:/bin:/usr/sbin:/usr/bin
LD_LIBRARY_PATH : /opt/xilinx/xrt/lib:
sh-4.2# ./helloworld xclbin/vector_addition.hw.xilinx_aws-vu9p-f1-04261818_dynam
ic_5_0.awsxclbin
xclProbe found 1 FPGA slots with xocl driver running
Found Platform
Platform Name: Xilinx
Found Device=xilinx_aws-vu9p-f1-04261818_dynamic_5_0
XCLBIN File Name: vector_addition
INFO: Importing xclbin/vector_addition.hw.xilinx_aws-vu9p-f1-04261818_dynamic_5_
0.awsxclbin
Loading: 'xclbin/vector_addition.hw.xilinx_aws-vu9p-f1-04261818_dynamic_5_0.awsx
clbin'
INFO: Could not load AFI for data retention, code: 18 - Loading in classic mode.
AFI load complete.
Result =
19 19 19 19 19 19 19 19 19 19 19 19 19 19 19 19
19 19 19 19 19 19 19 19 19 19 19 19 19 19 19 19
19 19 19 19 19 19 19 19 19 19 19 19 19 19 19 19
19 19 19 19 19 19 19 19 19 19 19 19 19 19 19 19
TEST PASSED
sh-4.2# ▌
```

Pipelining

The pipeling loop for the PCIe design provides less number of Execution cycles, real time hardware acceleration with data speed of PCIe x8 Gen 3 8GT/s, width x8.



```
  ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

Attempting to get a license: ap_opencl
Feature available: ap_opencl
INFO: [XOCC 60-585] Compiling for hardware emulation target
Running SDx Rule Check Server on port:43293
INFO: [XOCC 60-895]   Target platform: /home/centos/aws-fpga/SDAccel/aws_platform/xilinx_aws-vu9p-f1-04261818_dy
dynamic_5_0.xpfm
INFO: [XOCC 60-423]   Target device: xilinx_aws-vu9p-f1-04261818_dynamic_5_0
INFO: [XOCC 60-242] Creating kernel: 'vector_add'

===>The following messages were generated while  performing high-level synthesis for kernel: vector_add Log file
elloworld_ocl/_x/vector_addition.hw_emu.xilinx_aws-vu9p-f1-04261818_dynamic_5_0/vector_add/vivado_hls.log :
INFO: [XOCC 204-61] Option 'relax_ii_for_timing' is enabled, will increase II to preserve clock frequency constr
INFO: [XOCC 204-61] Pipelining loop 'Loop 1.1'.
INFO: [XOCC 204-61] Pipelining result : Target II = 1, Final II = 1, Depth = 3.
INFO: [XOCC 204-61] Pipelining loop 'Loop 1.2'.
INFO: [XOCC 204-61] Pipelining result : Target II = 1, Final II = 1, Depth = 3.
INFO: [XOCC 204-61] Pipelining loop 'vadd_writeC'.
INFO: [XOCC 204-61] Pipelining result : Target II = 1, Final II = 1, Depth = 3.
INFO: [XOCC 60-594] Finished kernel compilation
INFO: [XOCC 60-244] Generating system estimate report...
```

4 CONCLUSION

The IoT Based design will give the Optimized Solution and Diagnostics capabilities for the benefit of humans. The PSO Techniques and Fuzzy Interpretation using Cloud Processing help in saves thousands of lives. The Hardware platform gives real time on chip processing, real time hardware acceleration, Profiling report showes less number of execution cycles on PCLe based implementation. Virtual servers with the help of openCL/C++ libraries, Xilinx SDx Environments and virtual JTAG interfaces on Xilinx Virtex Ultrascale Plus Board(VU9P) low profile PCIe accelerated Board provides low latency and high performance software profiling solutions.

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