Average Modeling of Fly-buck Converter

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Keywords: Average Model, Fly-buck, Dc/dc Converter.

Abstract: This document presents an average macro model for the fly-buck converter. The model can be used for both large and small signal modeling. Parasitic and lossy components are included in the model, and it is partially based on a conventional average switch model for a buck stage. For isolated output, the analytic solution of the average current in a secondary winding is proposed. The presented model is implemented in SPICE, and simulation results are compared to switching model simulation and experimental data.

1 INTRODUCTION

The fly-buck converter has become popular because it has several advantages, such as good cross regulation, line transient response, and low EMI, (Fang and Meng, 2015; Karlsson and Persson, 2017; Gu and Kshirsagar, 2017; Choudhary, 2015; Nowakowski, 2012). It has a simple design and provides multiple isolated outputs. A small-signal analytical model for an ideal fly-buck converter was presented in (Wang et al., 2017), but the effects of component parasitics could not be predicted.

The proposed model can be used for both large and small signal analysis and can be simulated in time or frequency domains. The difficulty of developing such a model is that leakage inductance current has a pulsed shape and cannot be approximated with conventional small ripple approximation, (Erickson and Maksimovic, 2007). To overcome this issue, the current is calculated during the instantaneous switching period, and small ripple approximation is used for the transformer's magnetizing inductance current and capacitor voltages. The model accounts for the losses and parasitics of semiconductors and magnetics and has been implemented as a SPICE subcircuit. The following assumptions were considered: the model covers two isolated outputs, and the dead-time effect is negligible.

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2 MODEL DERIVATION

The fly-buck converter's basic structure is shown in Fig. 1. The MOSFETS Q_1 and Q_2 have on-state resistances R_{on1} and R_{on2}, respectively. The transformer T_1 has secondary side-related leakage inductance L_s, magnetizing inductance L_m, primary winding resistance R_{pri}, secondary winding resistance R_s, and turns ratio $1 : n$. The diode D_1 is modeled with on-state resistance R_D and forward bias voltage V_D. Components listed above are internal parts of the proposed model. The input voltage $v_{in}(t)$, output voltages $v_{out1}(t)$ and $v_{out2}(t)$, and the corresponding load networks (R_1/C_1 and R_2/C_2) are connected externally to the model. The converter has switching frequency $F_{sw} = 1/T$.

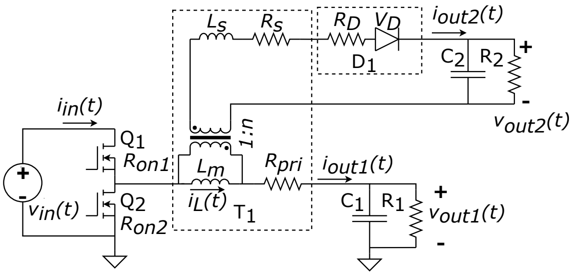

Figure 1: Fly-buck converter with two outputs.

The main waveforms are shown in Fig. 2. The switching period is divided into three parts, and the first interval d_1 is the time when leakage inductance L_s resets. The switch Q_1 is on, and the Q_2 is off. The diode D_1 is forward-biased. The second interval d_2 is the time when the diode D_1 blocks, Q_1 is on, and Q_2 is off. The third interval d_3 is the time

Zaikin, D., Mikkelsen, S., Jonasen, S. and Sirenko, K.
Average Modeling of Fly-buck Converter.
DOI: 10.5220/0007933703270331
In *Proceedings of the 9th International Conference on Simulation and Modeling Methodologies, Technologies and Applications (SIMULTECH 2019)*, pages 327-331
ISBN: 978-989-758-381-0

when Q_1 is off, Q_2 is on, and D_1 conducts. The duty cycle is determined as $d = d_1 + d_2$ and $1 - d = d_3$.

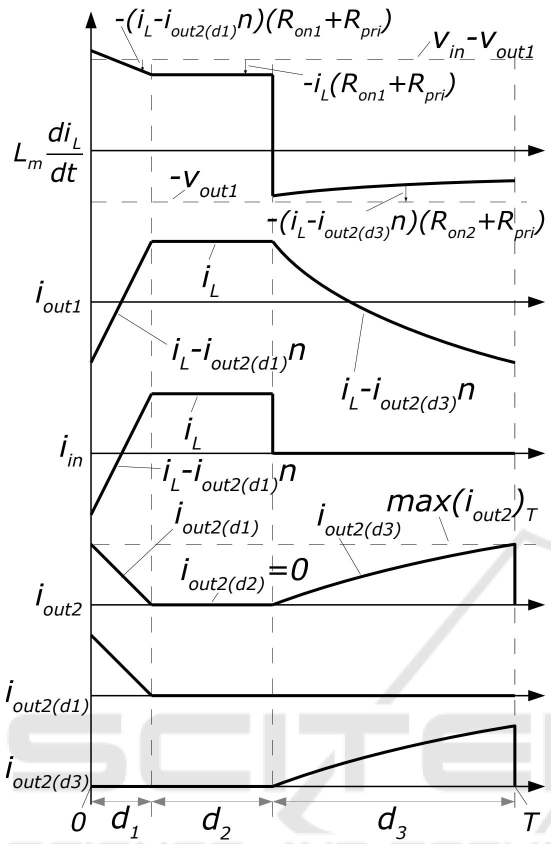

Figure 2: Waveforms of the fly-buck converter.

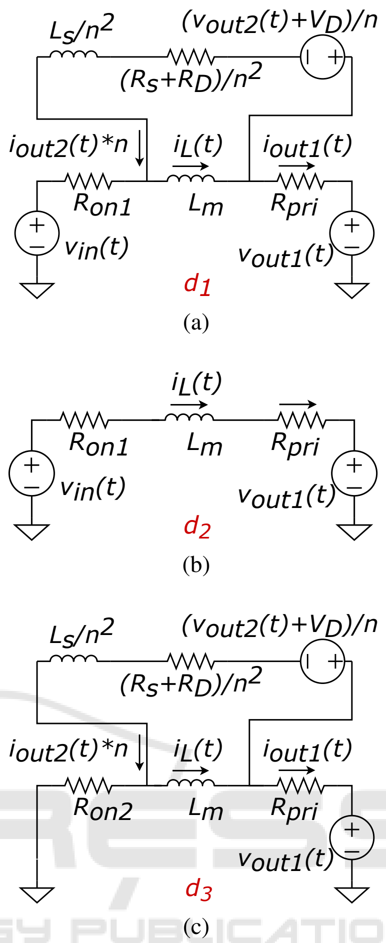

Figure 3: Equivalent circuits of the converter for different time intervals.

States of the converter at each time interval $d_1 - d_3$ are presented in Fig. 3. Using the small ripple approximation average, voltage across the inductor can be obtained:

$$
\begin{aligned}
L_m \frac{d\langle i_L(t)\rangle_T}{dt} &= \langle v_{in}(t)\rangle_T\, d - \langle v_{out1}(t)\rangle_T \\
&- \langle i_L(t)\rangle_T (R_{on1}\, d + R_{on2}\,(1-d) + R_{pri}) + \\
&\langle i_{out2_{(d_1)}}(t)\rangle_T (R_{on1} + R_{pri}) n + \\
&\langle i_{out2_{(d_3)}}(t)\rangle_T (R_{on2} + R_{pri}) n, \qquad (1)
\end{aligned}
$$

where $\langle x(t)\rangle_T$ represents the average value of x over the switching period T. The currents $i_{out2_{(d_1)}(t)}$ and $i_{out2_{(d_3)}(t)}$ are artificially shown in Fig. 2 separately, so $i_{out2}(t) = i_{out2_{(d_1)}}(t) + i_{out2_{(d_3)}}(t)$ due to $i_{out2_{(d_2)}}(t) = 0$. The average values of these currents will be obtained later.

By using the charge balance approach, the average currents for C_1 and C_2 can be found:

$$
C_1 \frac{d\langle v_{out1}(t)\rangle_T}{dt} = -\langle i_{out2}\rangle_T n - \langle v_{out1}(t)\rangle_T / R_1 + \langle i_L\rangle_T \qquad (2)
$$

$$
C_2 \frac{d\langle v_{out2}(t)\rangle_T}{dt} = -\langle v_{out2}(t)\rangle_T / R_2 + \langle i_{out2}(t)\rangle_T \qquad (3)
$$

The input voltage source's average current can be obtained as follows:

$$
\langle i_{in}(t)\rangle_T = \langle i_L(t)\rangle_T\, d - \langle i_{out2_{d1}}(t)\rangle_T\, n \qquad (4)
$$

To build the final model, the average currents $\langle i_{out2_{d1}}(t)\rangle_T$ and $\langle i_{out2_{d3}}(t)\rangle_T$ must be obtained. It can be seen from Fig. 2 that current $i_{out2_{d3}}(t)$ is an exponential process of magnetizing leakage inductance L_s. Fig. 3c can be used to find an analytical solution for the $\langle i_{out2_{d3}}(t)\rangle_T$ average current. The transient process during one switching period is considered. Variables $i_L(t)$, $v_{out1}(t)$ and $v_{out2}(t)$ can be replaced with constant sources for one switching period due to the small ripple approximation. The initial current in the L_s inductor is zero, so a solution for the peak and average currents can be found:

$$max(i_{out2})_T = \frac{E_{d3}(t)}{R_{d3}\, n}\left(1-e^{-\frac{R_{d3} n^2 t_{off}}{L_s}}\right) \tag{5}$$

$$\langle i_{out2_{d3}}(t)\rangle_T = \frac{E_{d3}(t)\, F_{sw}}{R_{d3}\, n}\left(\frac{L_s\left(1-e^{-\frac{R_{d3} n^2 t_{off}}{L_s}}\right)}{R_{d3}\, n^2}+t_{off}\right), \tag{6}$$

where $R_{d3} = R_{on2}+R_{pri}+(R_s+R_D)/n^2$, $t_{off} = (1-d)/F_{sw}$ and

$$E_{d3}(t) = \langle v_{out1}(t)\rangle + \langle i_L(t)\rangle\,(R_{on2}+R_{pri}) - \frac{(\langle v_{out2}(t)\rangle + V_D)}{n}.$$

A similar approach can be used to find $\langle i_{out2_{d1}}(t)\rangle_T$'s average current during the d_1 interval. Fig. 3a represents an equivalent circuit for this interval. Transient process of the leakage inductance reset is also considered in one particular switching period. The initial current in the L_s inductor is $max(i_{out2})_T$, found from (5), and then it resets to zero current. Thus, the solution is obtained as follows:

$$\langle i_{out2_{d1}}(t)\rangle_T = \frac{E_{d3}(t)\, F_{sw}\, L_s}{n^3\, R_{d1}\, R_{d3}}\left(1-e^{-\frac{n^2 t_{off} R_{d3}}{L_s}}\right) + \frac{E_{d1}(t)\, F_{sw}\, L_s}{n^3\, {R_{d1}}^2}\ln\left(1-\frac{E_{d3}(t)\, R_{d1}}{E_{d1}(t)\, R_{d3}}\left(1-e^{-\frac{n^2 t_{off} R_{d3}}{L_s}}\right)\right), \tag{7}$$

where $E_{d1}(t) = E_{d3}(t) - \langle v_{in}(t)\rangle - \langle i_L(t)\rangle\,(R_{on2}-R_{on1})$, $R_{d1} = R_{on1}+R_{pri}+(R_s+R_D)/n^2$. Using (1)–(3), the schematic of the fly-buck converter model can be constructed as shown in Fig. 4. The $\langle i_{out2_{d1}}(t)\rangle_T$ and $\langle i_{out2_{d3}}(t)\rangle_T$ currents ((6) and (7)) and realization of (3) are implemented by the Gd1 and Gd2 arbitrarily behavior current sources. The E3 source, along with L1, realizes (1). The G3 source is responsible for (4), while the G4 source implements (2). The ideal diodes D1 and D2 improve the convergence of the model by blocking negative voltages on the second output.

The model has next pins to connect to external circuits: node 'Vin' — input voltage, node 'Vout1' — first output (non-isolated), node 'Vout2' — second output (isolated) and node 'd' — duty cycle control input (0.0...1.0 range). The reference zero potential for the primary side is connected to the global '0' net, and the secondary side's ground potential is connected using a GND_SEC pin.

The sub-model netlist can be found in Fig. 5 and (Zaikin, 2019).

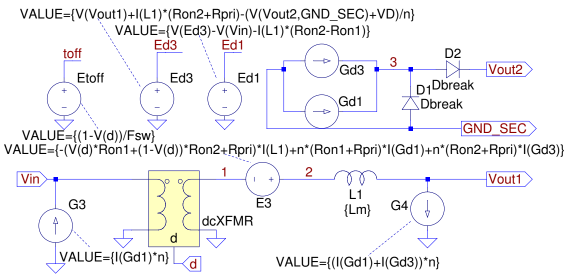

Figure 4: Fly-buck converter average model schematic.

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.SUBCKT FLY_BUCK_AVG Vin Vout1 Vout2 GND_SEC d
+PARAMS: Ron1=12m Ron2=12m VD=1.8 RD=0.2 Rs=0.07
+Ls=7.5u Rpri=10m Lm=3.8u n=5 Fsw=100k
.param Rd1={Ron1+Rpri+(Rs+RD)/n**2}
.param Rd3={Ron2+Rpri+(Rs+RD)/n**2}
L1 2 Vout1 {Lm}
Gd1 0 5 VALUE={(V(Ed1)*Fsw*Ls*log(1-(V(Ed3)*Rd1*
+(exp(-(Rd3*n**2*V(toff))/Ls)-1))/(V(Ed1)*Rd3)))/(Rd1**2*
+n**3)+(V(Ed3)*Fsw*Ls*(exp(-(Rd3*n**2*V(toff))/Ls)-1))/
+(Rd1*Rd3*n**3)}
Gd3 0 4 VALUE={(V(Ed3)*Fsw*(v(toff)+(Ls*(exp(-
+(Rd3*n**2*v(toff))/Ls)-1))/(Rd3*n**2)))/(Rd3*n)}
G3 0 Vin VALUE={I(Vd1)*n}
Ed1 Ed1 0 VALUE={V(Ed3)-V(Vin)-I(L1)*(Ron2-Ron1)}
Ed3 Ed3 0 VALUE={V(Vout1)+I(L1)*(Ron2+Rpri)-
+(V(Vout2,0)+VD)/n}
E3 2 1 VALUE={-(V(d)*Ron1+(1-V(d))*Ron2+Rpri)*I(L1)+
+n*(Ron1+Rpri)*I(Vd1)+n*(Ron2+Rpri)*I(Vd3)}
G4 Vout1 0 VALUE={(I(Vd1)+I(Vd3))*n}
D1 0 3 Dbreak
Etoff toff 0 VALUE={(1-V(d))/Fsw}
D2 3 Vout2 Dbreak
Vd3 4 3 0
Vd1 5 3 0
EdcXFMR 6 0 VALUE={V(Vin)*V(d)}
GdcXFMR Vin 0 VALUE={I(VdcXFMR)*V(d)}
RpdcXFRM Vin 0 1MEG
RsdcXFRM 1 7 1u
VdcXFMR 6 7 0
.ends FLY_BUCK_AVG
.model Dbreak D Is=1e-14 Cjo=.1pF Rs=1m N=0.01
```

Figure 5: The fly-buck converter LTSpice/PSpice sub-model netlist. Copy-paste is possible from pdf version of this paper.

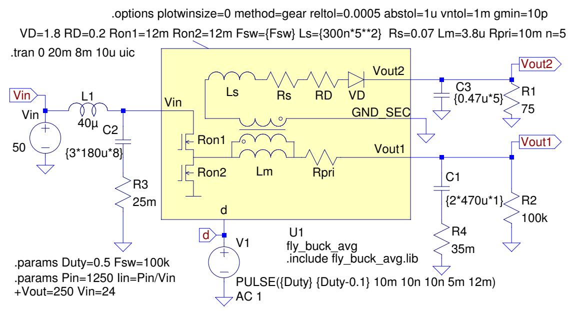

Figure 6: Fly-buck converter simulation setup.

3 RESULTS

The proposed model was simulated and compared to switching modeling, along with prototype measurement. The parameters for simulation and testing were $V_D = 1.8$ V, $R_D = 0.2$ Ohm (C3D06060A two in series), $R_{on1} = R_{on2} = 12$ mOhm (IPB117N20NFD), $F_{sw} = 100$ kHz, $Ls = 7.5$ uH, $Rs = 0.07$ Ohm, $Lm = 3.8$ uH, $Rpri = 10$ mOhm, and $n = 5$. The external circuit contained the input cable's 40 uH inductance, and capacitance at the input was 7.92 mF (25 mOhm ESR), R_1=100 kOhm, C_1=940 uF (35 mOhm ESR), R_2=75 Ohm, C_2=2.35 uF and the input voltage v_{in}=50 V. The circuit for simulation and measurement is shown in Fig. 6. The simulation results are presented in Fig. 7 and Fig. 8.

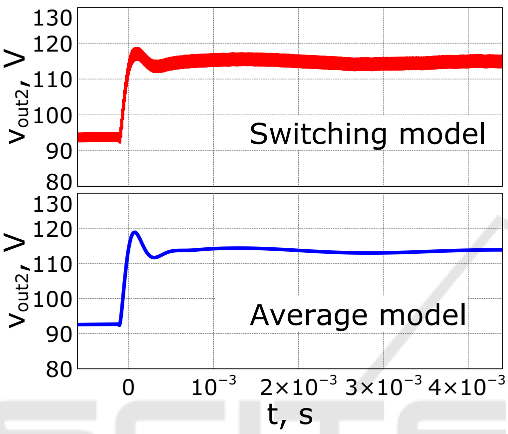

Figure 7: Simulation results. The v_{out2} step response on the duty cycle changed from 0.4 to 0.5.

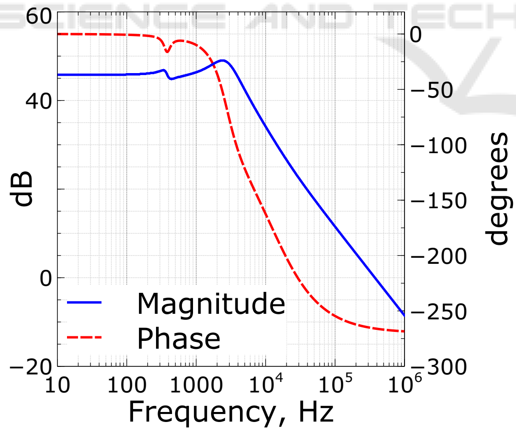

Figure 8: Simulation results. The transfer function $\frac{\hat{v}_{out2}(f)}{\hat{d}(f)}$ of the output voltage compared to a control.

The setup for testing is shown in Fig. 9. The measurement results are presented in Fig. 10.

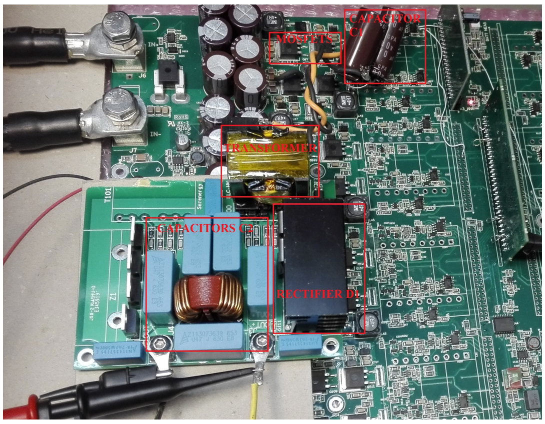

Figure 9: Fly-buck converter test setup.

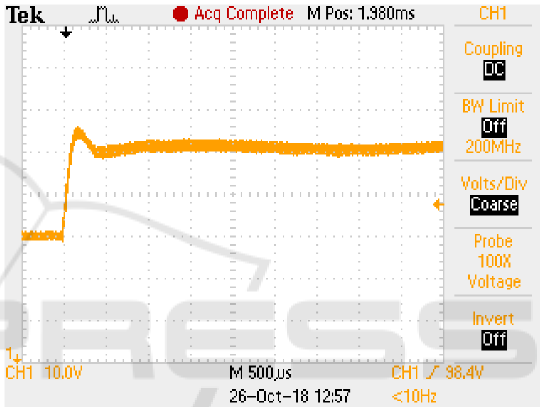

Figure 10: Measurement results. The v_{out2} step response on the duty cycle changed from 0.4 to 0.5.

4 CONCLUSION

The proposed model can be simulated for large and small signal modeling in time or frequency domains. The model accounts for parasitics of semiconductors and magnetics so losses and precise behavior can be predicted. A listing of the SPICE model was presented and it can be used for the static and dynamic behavior analysis of the fly-buck converter.

REFERENCES

Choudhary, V. (2015). Designing isolated rails on the fly with fly-buck^{TM} converters.

Erickson, R. W. and Maksimovic, D. (2007). *Fundamentals of power electronics*. Springer Science & Business Media.

Fang, X. and Meng, Y. (2015). Isolated bias power supply for igbt gate drives using the fly-buck converter.

In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2373–2379.

Gu, D. and Kshirsagar, P. (2017). Compact integrated gate drives and current sensing solution for sic power modules. In *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 5139–5143.

Karlsson, M. and Persson, O. (2017). Isolated fly-buck converter, switched mode power supply, and method of measuring a voltage on a secondary side of an isolated fly-buck converter. US Patent 9,755,532.

Nowakowski, R. (2012). Techniques for implementing a positive and negative output voltage for industrial and medical equipment. *How2Power Today*, pages 1–6.

Wang, W., Lu, D., Chai, Q., Lin, Q., and Cai, F. (2017). Analysis of fly-buck converter with emphasis on its cross-regulation. *IET Power Electronics*, 10(3):292–301.

Zaikin, D. I. (2019). Files for simulation. https://goo.gl/EUfctH. Accessed: 2019-03-24.